High Order Mismatch Shaping for Low Oversampling Rates

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Abstract— **Delta Sigma data converters employing high order dynamic element matching (DEM) allow for accurate signal conversion in the presence of DAC mismatch. However, at low oversampling rates, current high order DEM decoders provide little or no improvement in error suppression over lower order designs. In addition, the logic requirement of the DEM decoder increases significantly with each additional DAC bit. This paper presents a high order DEM decoder that improves mismatch shaping performance at low to medium oversampling rates by up to 15dB, while employing methods to reduce the area overhead of the vector quantizer in the design.**

Index Terms— **ADC, DAC, Decoder, Delta Sigma ($\Delta\Sigma$), DEM, Dynamic Element Matching, Element Selection Logic, Mismatch shaping, Oversampling.**

I. INTRODUCTION

DELTA sigma data converters employ oversampling and noise shaping to increase converter resolution and reduce analog circuit complexity. However, these converters rely on a highly linear DAC in the signal path, consequently any mismatch between the DAC levels leads to a degradation in the overall converter performance. Fortunately, multi-bit unary weighted DACs possess redundancy in terms of the elements that can be selected to form the DAC output. Combining this with the additional bandwidth afforded by oversampling means that dynamic element matching (DEM) can be employed to reduce the effects of mismatch error, effectively linearizing the DAC in the signal band. The extent to which mismatch error is reduced depends on the order of the DEM decoder and the oversampling rate at which it operates.

First order DEM [1] shapes the in-band mismatch error pushing it to higher frequencies. Second order DEM schemes [2] improve shaping performance and reduce tonal behavior. Second order schemes may also be optimized for low oversampling rates to increase signal bandwidth [3], however, this results in a reduction of the in-band error suppression. Moving from a lowpass to a bandpass DEM doubles the order of the DEM as the number of poles in the transfer function is doubled. However, this does not increase the order of the

shaping, rather it allows the DEM to shape the mismatch error around a center frequency. Bandpass DEMs may also be optimized for lower oversampling rates [4], but as in the case of the lowpass DEM this optimization trades a reduction in in-band error suppression for an increase in signal bandwidth.

Moving to higher order DEM designs yields greater suppression of the mismatch error giving us the potential to maintain a high level of error suppression over a wide bandwidth. However, realizing DEM designs of order >2 in lowpass and >4 in bandpass is difficult to achieve. In [5], the authors outline the use of a $\Delta\Sigma$ modulator structure to provide high order mismatch shaping in a vector feedback DEM design. Sun et al. [6] detail a significant advancement with the development of a 4th order lowpass vector feedback DEM.

Current high order DEM schemes suffer from two limitations. Firstly, they require a significant increase in hardware overhead and complexity when compared to lower order approaches. Secondly, current high order DEMs provide little or no improvement in performance at low to medium oversampling rates when compared to lower order DEMs. This paper attempts to address these issues by presenting a 4th order lowpass DEM design that provides better suppression of the mismatch error at low to medium oversampling rates. In addition to this, a method to reduce the area overhead by splitting the DEM is presented.

In section II we examine the selection of elements by DEM decoders and show why at low oversampling rates, conventional high order DEMs do not achieve an improvement in mismatch shaping when compared to lower order designs. The analysis focuses on lowpass DEMs but is equally valid for bandpass DEMs. Section III details the proposed design for a 4th order lowpass DEM decoder optimized for low to medium oversampling rates. Section IV describes a method to reduce the logic area of the decoder. Finally, section V contains a short summary of this brief.

II. ANALYSIS OF MISMATCH SHAPING

The objective of a DEM decoder is to select the DAC elements so that the mismatch error is shaped out of band. The mismatch shaping transfer function is given by $(1-z^{-1})^L$ where L denotes the order. A general model for mismatch shaping is given in [7], the authors show that mismatch shaping of any order can be realized by a series of thermometric conversions described by (1). Where a_j represents the coefficients of the mismatch transfer function, e.g. for 1st order mismatch shaping $(1\text{-}z^{-1})^1$ $a_0 = 1$, $a_1 = -1$. For 2nd order mismatch shaping $(1\text{-}z^{-1})^2$ $a_0 = 1$, $a_1 = -2$, $a_2 = 1$. ptr represents the pointer to the elements in the

array. $c[k]$ represents an overflow operation, whereby all the elements in the DAC array contribute to the output based on the value of $c[k]$. M is the number of elements in the DAC and w_i for $i = 0$ to $M - 1$, represents the weights of the individual DAC elements.

$$y[k] = c[k] \cdot \sum_{i=0}^{M-1} w_i + \sum_{j=0}^{L} a_j \cdot \left(\sum_{i=0}^{ptr[k-j]-1} w_i \right) \qquad (1)$$

Equation 1 shows it is possible to construct a mismatch shaping transfer function of arbitrary order using the appropriate filter coefficients. However, for orders greater than 1, the DAC must have the following properties:

1) Each DAC element must be able to contribute positively, negatively or have zero contribution during a conversion cycle
2) Each DAC element must be able to contribute multiple times during a conversion cycle

It is possible to construct a DAC with these properties using pulse density modulated elements clocked at multiples of the oversampling rate [8]. However, operating the DAC at multiples of the oversampled rate is difficult to achieve and limits the application to lower order DEMs.

For most noise shaping converters, the elements in the DAC operate at the oversampling rate and only contribute to the output in two ways i.e. (1, 0) or (1, -1). Consequently, any mismatch shaping algorithm applied to the DAC must be limited to selecting the elements once during each conversion cycle. This limit does not prevent the implementation of higher order mismatch shaping, however, as shown in Fig. 1, it results in the frequency response of the DEM deviating from the ideal. Due to the limit on element selection, the frequency response of high order DEMs flattens out at high frequencies, which results in an increase in the error contribution at lower frequencies. This alteration in frequency response means that when operating at large oversampling rates high order DEM decoders provide excellent suppression of the mismatch error, however, at low oversampling rates, conventional high order DEM designs offer little or no gain in SNR performance when compared to low order DEM decoders.

III. PROPOSED DEM DESIGN

To increase the performance of high order mismatch shaping at lower OSRs, the proposed design employs a 4th order mismatch shaper that distributes the error more evenly across the signal band, sacrificing error suppression at OSRs >32, to achieve greater suppression at OSRs between 8 and 32. The design uses a vector feedback DEM as described in [9]. This DEM structure was chosen as it allows us to exploit techniques used in $\Delta\Sigma$ modulator design to select and tune the desired mismatch transfer function (MTF). The vector feedback DEM structure resembles that of a conventional modulator, however, instead of employing a single loop filter to shape the noise, the DEM consists of M mismatch shaping filters in parallel. The filters share a common quantizer in the form of a vector quantizer (VQ). The VQ chooses which DAC elements to activate based on the filter values at its inputs. The
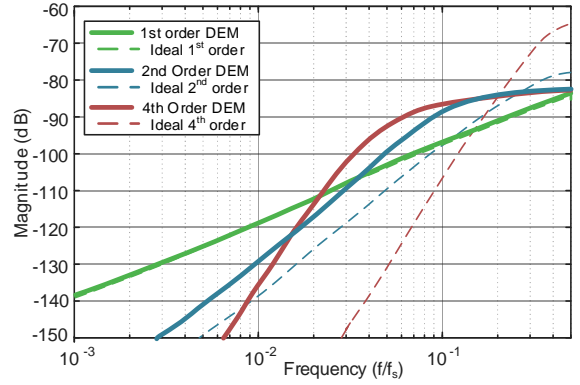

Fig. 1. Frequency response of 1st, 2nd and 4th order mismatch shaping.

M parallel outputs of the VQ that control the DAC elements are also used to provide feedback signals to the mismatch shaping filters.

A. Mismatch filter transfer function

Conventional vector feedback DEMs employing FIR filters are limited to mismatch shaping orders ≤ 2 for lowpass, or ≤ 4 for bandpass DEMs. Higher order mismatch transfer functions are prone to instability, due to the high out of band gain causing the VQ to saturate. To overcome this limitation, the proposed DEM is reconfigured so that the outputs of the VQ are directly filtered using IIR filters. The filters as shown in Fig. 2 are realized by cascading four integrator stages with coefficients placed around the loop to create the desired 4th order lowpass MTF. The filters can also be reconfigured to realize an 8th order bandpass MTF centered at Fs/4, by placing an extra delay in each of the integrator stages.

To maintain stability, the out of band gain of the filter at high frequencies is reduced by moving the poles closer to DC. To improve mismatch error suppression at low oversampling rates, the locations of the zeros are distributed along the unit circle, creating notches in the filter response. Within the filter, the input signal is distributed to each integrator stage through the coefficients a_1 to a_4. The inter-stage coefficients c_1 to c_4 scale the outputs of the integrator stages to maintain dynamic range, while the feedback coefficients g_1 and g_2 are used to optimize the zero locations. To generate a set of suitable filter coefficients, a multistep optimization approach is used. For the first step, Butterworth and inverse Chebyshev filter transfer functions are used to generate initial values for the pole zero locations. Starting with these values, a series of Monte Carlo simulations are performed to find the bounds of the pole zero locations that represent stable MTFs. Next, a random walk optimization is used to explore the space within the region of stable MTFs, the objective of the optimization is to find an MTF that yields the best mismatch error suppression over the desired signal band, while minimizing the values at the output of the integrator stages. This minimization objective is important as it significantly reduces the bit width of the filters when compared to other designs [6]. From this subset of MTF's, a set of coefficients that can be readily implemented using shift and add operations is chosen. This procedure allows for an optimal tradeoff between mismatch shaping performance, stability, and area overhead.
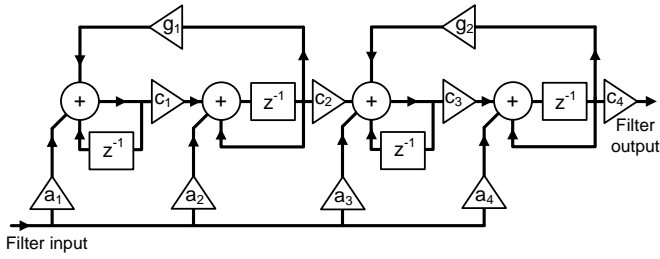
Fig. 2. Mismatch shaping filter implemented using cascade of integrators structure

B. Mismatch shaping performance

Fig. 3(a) compares the frequency response of the proposed DEM to that of a conventional 4th order DEM [6]. The conventional 4th order DEM provides very high suppression of the mismatch error at low frequencies (high OSRs), while the proposed design spreads the mismatch error more evenly over the signal band. This allows the DEM to maintain error suppression over a wider bandwidth, giving a significant improvement in SINAD performance at lower OSRs. Fig. 3(b) shows the frequency response of the DEM when operating in an 8th order bandpass configuration. When compared to a 4th order bandpass DEM, the additional poles in the mismatch shaping filters of the proposed design provide more suppression of the mismatch error around the signal band.

To assess mismatch shaping performance, the proposed DEM is simulated using a 5th order low pass $\Delta\Sigma$ modulator designed to operate over a wide bandwidth. The DEM is applied to a 5-bit DAC, comprising of 32 unary weighted elements with 1% mismatch error. Fig. 4 plots the frequency response of the proposed design with a 4th order DEM [6] and a 2nd order DEM optimized for low OSR [3]. At high OSRs the conventional 4th order DEM suppresses the mismatch error below the converter noise floor. This makes the 4th order DEM suitable for converters operating at OSRs greater than 32. However, as the signal bandwidth increases the 4th order DEM contributes more mismatch error leading to a reduction in SINAD performance. The 2nd order DEM optimized for low OSR exhibits an approximately flat spectrum over the converter bandwidth, allowing the DEM to maintain a constant SINAD value over a range of OSRs. However, the increase in bandwidth comes at the cost of greater error contribution at lower frequencies.

The proposed 4th order filter spreads the mismatch error across a larger signal band, allowing the DEM to maintain a higher level of error suppression at low frequencies when compared to the 2nd order DEM. In addition, the sharp transition band of the filter means that at lower OSRs the proposed DEM contributes less error than the conventional 4th order DEM. Table I compares the SINAD values for all three designs operating at OSRs 8 – 32. The results show that at an OSR of 8 and 32, the performance of the proposed DEM is comparable to the 2nd and 4th order DEMs respectively. For OSRs less than 32 and greater than 8, the proposed DEM maintains a higher SINAD performance compared to the 4th and 2nd order DEMs, demonstrating >15dB improvement at an OSR of 16.
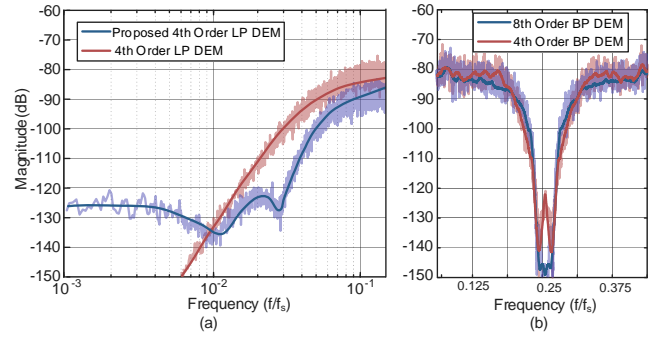

Fig. 3. (a) Spectrum of mismatch error of proposed DEM and conventional DEM operating in lowpass configuration. (b) Spectrum of mismatch error of proposed DEM and conventional DEM operating in bandpass configuration
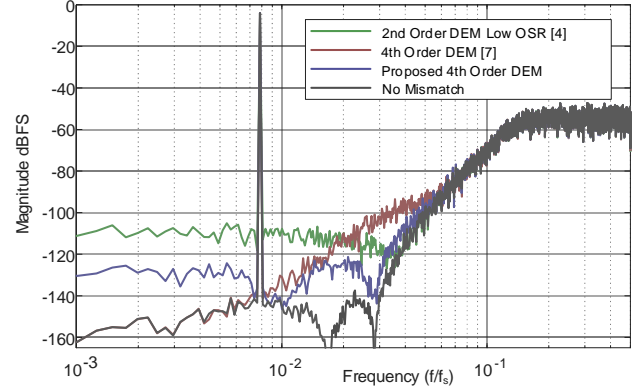

Fig. 4. Frequency response of DAC output with 1% mismatch for 2nd order, 4th order and proposed DEM design.

TABLE I
SINAD/SFDR (DECIBEL) COMPARISON FOR 1% MISMATCH ERROR

OSR	This work SINAD/SFDR		4th Order DEM [6] SINAD/SFDR		2nd Order DEM [3] SINAD/SFDR	
32	107	121	109	122	90	107
28	105	120	102	116	90	106
24	104	119	98	108	89	105
20	104	119	93	103	88	105
16	103	118	86	100	87	104
12	90	103	78	94	87	104
8	71	85	68	85	73	86

IV. REDUCED HARDWARE DEM

The vector feedback DEM structure requires the VQ to sort the outputs of the filters in a single conversion cycle. To achieve this fast sorting, the VQ is implemented as an array of comparators as shown in Fig. 5. The first stage of the VQ comprises of $(M^2 - M)/2$ comparators, where M represents the number of DAC elements. The outputs of the first stage are added using M n-bit adders, where $n = log_2(M)$. The final stage compares the outputs of the adders to the modulator value using M n-bit comparators. Since the number of comparators required doubles for each additional DAC element, this makes the VQ a significant portion of the design. Previous designs [10] have sought to reduce the complexity of the VQ by partially sorting the outputs of the mismatch shaping filters. While this leads to a saving in the hardware overhead, it also leads to a reduction in the SNR and stability of the DEM [6]. Consequently, it is not suitable for high order DEM schemes operating at low oversampling rates.

To reduce the size of the VQ, the proposed design splits the DEM into two sub DEM decoders, each controlling $M/2$ DAC

elements. While the DEM now requires two VQs, a breakdown of the logic overhead as detailed in Table II shows that implementing both VQs, each operating on $M/2$ elements requires approximately half the number of gates compared to a single VQ operating on M elements. Fig. 5 shows an example of an 8 element split DEM, with the breakdown of the gate count given in Table III.

Splitting the DEM requires the input signal $x[k]$ to be divided into two sub signals $x_a[k]$, $x_b[k]$, which are then applied to the sub DEM decoders as shown in Fig. 5. This split or cascaded DEM design requires that the mismatch error between the sub DEM decoders does not leak or fold back into the signal band. The scheme described in [11] uses a DWA type flipper to split the signal among the sub DEM decoders. While the scheme allows the mismatch error between the sub DEM decoders to be shaped out of band, the DWA type flipper gives rise to tones and is not sufficient to maintain mismatch shaping for DEMs of order >2, or DEMs operating at low oversampling rates.

To provide cancellation of the mismatch error between the sub DEM decoders, the proposed DEM uses a modified switching block similar to that employed in the tree structure DEM [12]. This splits the modulator output $x[k]$ and ensures that the signals in $x_a[k]$ and $x_b[k]$ are sufficiently shaped to cancel the mismatch error between the sub DEM decoders.

The switching block operates by dividing $x[k]$ between the output paths $x_a[k]$, $x_b[k]$ while controlling the assignment of the remainder using an independent noise shaping loop. On each conversion cycle, if the input to the switching block is even, the output of the noise shaping loop $s[k]$ is set to zero. If the input to the switching block is odd, the noise shaper sets $s[k]$ to +1 or -1 depending on the current state of the loop filter. The outputs of the switching block ($x_a[k]$, $x_b[k]$) are formed by combining $s[k]$ with $x[k]$ as shown in Fig. 5. This allows the switching block to deterministically assign the remainder to one of the output paths so that the sequences $x_a[k]$ and $x_b[k]$ are noise shaped.

Using a tree structure DEM that employs a sequence generator with 2 levels is prone to instability [4]. To overcome this, the design uses a modified switching block that generates a noise shaped sequence on both odd and even valued inputs. Within the switching block, two quantizers with different step sizes are used. The "odd" quantizer has a step size $\Delta = 1$, quantizing the filter output to (1, 0, -1). The "even" quantizer has a step size $\Delta = 2$, quantizing the filter output to (2, 0, -2). A mux controlled by the LSB of $x[k]$ chooses which quantizer value is placed on the sequence $s[k]$. The dual quantizer configuration gives a multi-bit output and facilitates shaping on both even and odd input values. This allows the sequence generator to remain stable over a larger range of input amplitudes. Additionally, as in the case of $\Delta\Sigma$ modulator design, a multi-bit quantizer significantly improves SNR performance and allows 2nd or higher order filters to be used to split the DEM input signal. The combination of higher order filtering and multibit output reduces the potential of the output sequences $x_a[k]$, $x_b[k]$ becoming correlated with $x[k]$, thus significantly improving tonal behavior.
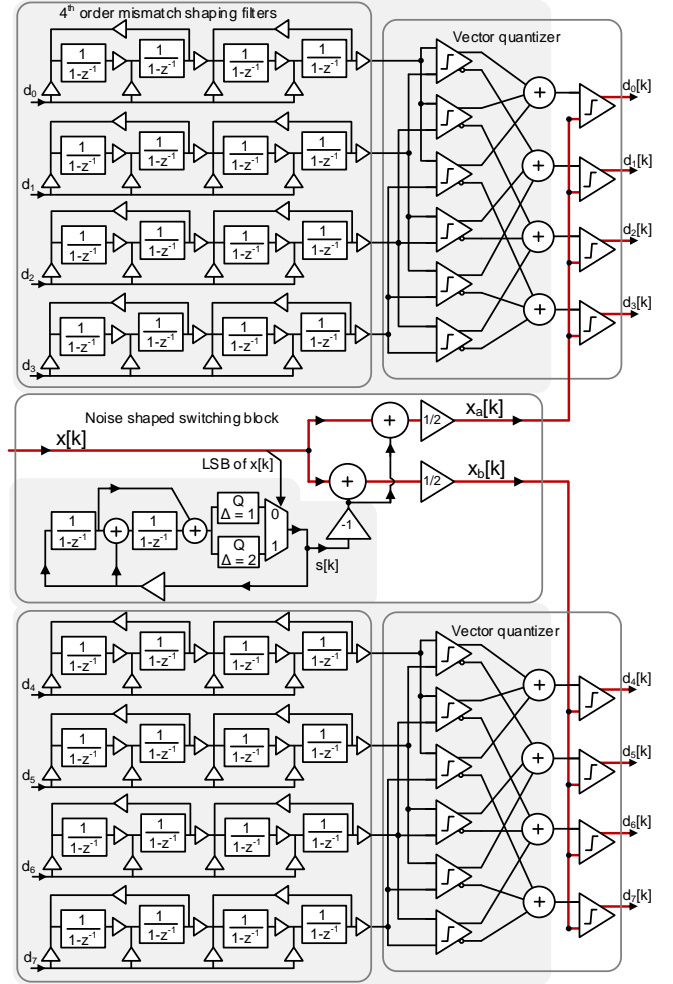

Fig. 5. Implementation of 8 element split DEM decoder employing 4th order mismatch shaping.

TABLE II
ESTIMATED GATE COUNT FOR SPLIT AND NON-SPLIT VQ

VQ design	Logic unit	# Units	Est ND2 gates	Total
Non split	8-bit comparator	28	2800	
	3-bit adder	8	192	
	3-bit comparator	8	384	3376
Split	8-bit comparator	12	1200	
	2-bit adder	8	128	
	2-bit comparator	8	256	1584

TABLE III
ESTIMATED GATE COUNT FOR 8 ELEMENT 4TH ORDER DEM DECODER

DEM	Logic unit	# Units	Est ND2 gates	Total
	4th order filter	8	6768	
	Switching block	1	75	
	Vector Quantizer	2	1584	8427

Splitting the DEM as shown in Fig. 5 results in each sub DEM controlling a set of $M/2$ DAC elements. Each sub DEM must shape the error power σ^2 contained in the set of elements it controls. The error power denoted as σ_a^2 and σ_b^2 is determined by the variance of the elements contained in the set as shown in (2), where e_i represents the mismatch error on an element.

The splitter block is responsible for shaping the error

between the two sets of elements. This error σ_{ab}^2 is the variance of the mean value of each set of elements, as shown in (3).

$$\sigma_a^2 = Var\{e_0, e_1, \dots, e_{\frac{M}{2}-1}\}, \ \sigma_b^2 = Var\{e_{\frac{M}{2}}, e_{\frac{M}{2}+1}, \dots, e_{M-1}\} \quad (2)$$

$$\sigma_{ab}^2 = Var\{\mu_a, \mu_b\}, \ where$$

$$\mu_a = \frac{1}{M/2}\left(\sum_{i=0}^{\frac{M}{2}-1} e_i\right), \ \mu_b = \frac{1}{M/2}\left(\sum_{i=\frac{M}{2}}^{M-1} e_i\right) \quad (3)$$

Due to this averaging effect, the error power σ_{ab}^2 will be $M/2$ times less than the error power in each set of elements (σ_a^2, σ_b^2). Consequently, while the modified splitter block allows for a high order filter to be used in the sequence generator, it is not always necessary due to the improved shaping provided by the dual quantizer. Fig. 6 compares the SINAD and SFDR for a split and non-split DEM using a 32 element DAC with 1% mismatch error for 100 simulation trials. The values show a 2-3dB loss in SINAD when compared to the non-split DEM. The mismatch used during the trials is randomly distributed. However, if the mismatch has a gradient distribution, the error between the sub DEMs will be larger due to the spatial difference between the two sets of elements controlled by the sub DEMS. To mitigate against this, the sub DEM blocks may be interleaved, where the first sub DEM controls odd numbered elements and the second sub DEM controls even numbered elements.

Using the DEM decoder in the feedback path of an ADC requires minimizing the delay through the DEM, as excess loop delay will lead to instability. While the high order DEM requires a significant logic overhead, the majority of the decoder logic as indicated by the shaded area in Fig. 5 operates outside of the critical input-output path. Consequently, these logic blocks have a full conversion cycle to execute and do not directly add to the delay through the DEM. The input-output path of the DEM decoder is highlighted in red in Fig. 5. The input signal $x[k]$ passes through an n-bit adder and a n-bit comparator before emerging as the set of 1-bit signals used to control the DAC elements. This leads to a relatively small propagation delay through the DEM, making it suitable for shaping the DAC mismatch in the feedback path of an ADC.

V. CONCLUSION

This paper presented the analysis and design of a DEM decoder targeted at low oversampling rates. The analysis showed how constraints placed on the DEM by the DAC leads to a reduction in the performance of high order DEM decoders at low oversampling rates. To improve performance at low OSRs, the DEM design in this paper employs a 4th order mismatch shaping filter in a vector feedback DEM architecture. The filter transfer function is designed to provide greater levels of mismatch error suppression at low oversampling rates. The proposed DEM exhibits better SINAD performance when compared to conventional high order DEM decoders for OSR values 8-32. Finally, a
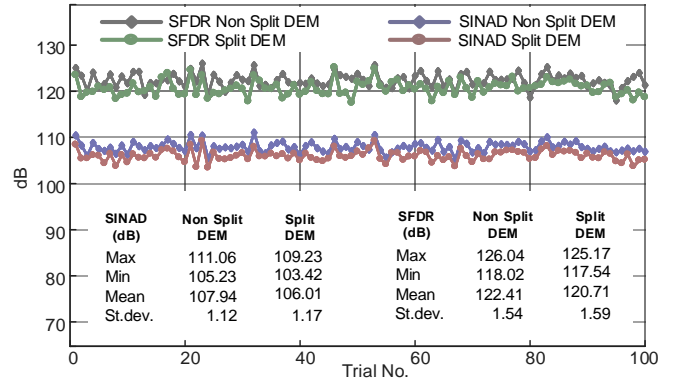

Fig. 6. SFDR/SINAD values of split and non-split 4th order 32 level DEM with 1% random mismatch error simulated over 100 trials.

technique to reduce the area overhead of the VQ in the DEM decoder was presented. The design uses a modified switching block to split the DEM into two sub DEM decoders, allowing the total area required by the VQs in the DEM to be halved.

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