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Performance Investigation of FinFET Based MO-CCII and its applications: Resistor-less Multi-Function Bi-quadratic Filter and Balanced Modulator

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This paper presents an optimal design of a high-performance multi output second-generation current conveyor (MO-CCII) based on 20nm FinFETs. Proposed MO-CCII has very low port X impedance and very high port Y impedance. The performance of the CCII has been thoroughly investigated in terms of DC, AC and transient characteristics of terminal voltages and branch currents and frequency response of port impedances. CCII shows the excellent high-frequency response of voltage as well as current transfer gains. The 3dB BW of voltage and current transfer gains are 11.2GHz and 11GHz respectively. CCII provides excellent performance over its CMOS counterpart. Also, a resistor-less multi-function bi-quadratic filter is proposed. The filter depends on two CCIIs, a capacitor and does not require any resistors. It has three inputs and one output and realizes low-pass, high-pass and band-pass filters from a similar setup. FinFETs in the linear region are utilized as variable resistor to control filter properties. Nevertheless, the proposed filter has two floating capacitors which can be effortlessly realized in these days' integrated circuit advancements. Also, a balanced modulator is proposed utilizing the proposed FinFET based CCII and FinFET transistors only. Balanced modulator's frequency of operation obtained is in GHz range.

Keywords: Balanced Modulator, Current Conveyor, Current Mode Circuits, FinFET, Multi-Function Biquadratic Filter

1. Introduction

The ongoing tremendous progress of semiconductor fabrication technology has permitted speed trends in the shrinkage rate of integrated circuits' (IC's) die area.

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As per,[1] in 2017, there was created a chip in 10nm CMOS process node with the thickness of 100million transistors per $1mm^2$. Such an integration density brings extraordinary improvement of computational power per area. However, this pattern brings additional disadvantage, as downscaled process node endures from the random fluctuation of process parameters, voltage and temperature sensitivity (PVT) along with various samples on a wafer.[2–4]

With the requirement of highly down-scaled transistors in state-of-the-art ICs, lower power consumption, high performance and battery operated systems, CMOS circuits faced many challenges like Short Channel Effects (SCEs), process variations, *etc.*[5]

The techniques used for low power design are Self-Cascode topologies, MOS transistors operating in the sub-threshold region, gm/I_D approach, Bulk-Driven (BD) MOS transistors, Dynamic-Threshold MOS (DTMOS) transistors, *etc.* But these techniques provide low power design for lower frequencies and lower speed.[6–9]

Below 22nm transistor technology, FinFET devices become the prominent alternative to the Bulk CMOS as they can easily be integrated with the CMOS ICs and reduce SCEs. Also, they can provide better high frequency response as well as higher speed when compared with CMOS.

Introduction of multi-Gate devices such as FinFETs created a revolution in the VLSI industry. As bulk CMOS faces many SCEs when scaled down below 22nm transistor technology, it becomes necessary to have a new device which can reduce these SCEs. Some of the SCEs are Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Leakage (GIDL), velocity saturation, hot carrier effect, *etc.* FinFETs, on the other hand, can restrict these SCEs because of better Gate control over the drain current (I_D) to provide lower voltage and low power operation of the device. Also, FinFET based devices are much faster and consume lower dynamic as well as static power when compared with bulk CMOS. In this paper, 20nm PTM model of FinFET has been used, which is discussed in.[10]

In the course of recent years, there has been a developing enthusiasm for Current-Mode (CM) circuits. In contrast with traditional Voltage-Mode (VM) signal processing, there are various advantages to pick up from CM circuits, for example, low voltage operation, great frequency performance, substantial dynamic range, higher bandwidth (BW), simpler architectures, lower power consumption, *etc.* In the expansion, innovative solutions gave by CM approach help designers to take care of the issues of the circuit design in modern technologies. Nowadays, extensive research has been done in this field to use various CM active building blocks and substitute VM circuits by CM ones. In recent years many applications based on CM circuits have been implemented like oscillators, filters, instrumentation amplifiers, impedance converters, *etc.*[11–15] Clearly, the most utilized CM active building blocks are current conveyors (CCs).[16]

There is a need for a basic building block that can be used to implement the different type of analog functions. One such block is Operational Amplifier (OPAMP)

that can be used to implement a large number of analog functions. It is a VM circuit and has suffered from the constant gain-BW product, poor slew rate, poor high-frequency response, lower BW, *etc.* CCII can be a real competitor of OPAMP, because it is a CM device, and has many advantages over OPAMP like higher BW, better slew rate, lower power consumption, larger dynamic range, *etc.*

Initially, analog building blocks like OPAMPs, Operational Transconductance Amplifiers (OTAs), CCs, *etc.* were designed using BJTs. BJTs have many advantages like large gain-BW product, better high-frequency performance, better voltage gain, high current density, high driving capability, *etc.* On the other hand BJTs have many disadvantages, like large associated noise, radiation effects, consume large power, very low thermal stability, *etc.* But as circuit complexity starts increasing BJTs consume very large power. So, IC industry started searching for other devices and came up with MOSFETs. Because they produce very low noise, better thermal stability, simpler to fabricate, higher integration density, and consume very low power. But as technology scaling goes beyond 22nm technology node CMOS implementation of ICs also affected by many effects like SCEs, sub-threshold leakage, *etc.*, some of the new techniques like Carbon Nano Tube Field Effect Transistors (CNTFETs), FinFETs, Tunnel FETs (TFETs), *etc.* were developed. But IC industry mainly used FinFETs as an alternative to CMOS, because they are compatible with CMOS process and by adding a small number of steps in CMOS process flow, FinFET based circuits can be implemented easily.

This paper is organized into seven sections. Section II presents an overview of FinFET devices. Section III highlights important aspects of a current conveyor. In Section IV performance of the FinFET based CCII has been investigated using HSPICE. Section V presents theory and simulation results of MO-CCII based multifunction bi-quadratic filter. In section VI, theory and simulation results of proposed balanced modulator are present followed by conclusions drawn in Section VII.

2. FinFET Overview

Difficulty in the fabrication of Double Gate MOSFET (DGMOS), because of the alignment problem of front and back gates, there is a need for an alternative technology which can overcome this problem. The development of FinFET (Fin-Shaped Field Effect Transistor) overcome these fabrication problems of DGMOS. The gate region covers the body from three sides. FinFET is a Non-planar Multi-Gate device mounted on a Silicon on Insulator (SOI) substrate which reduces the off current (I_{OFF}) to reduce static power consumption. The basic structure of FinFET is shown in Fig. 1a. Channel in FinFET is a semi-conducting fin which has a width w and height h, where $w< h$. The distance between source and drain of FinFET is known as fin length (L). Fin height (H_{FIN}) and fin thickness (T_{FIN}) are the main characteristics of a fin. The SOI substrate provides many advantages over Bulk CMOS like lower I_{OFF}, lower operating voltage, no drain current losses due to body effect, better control of gate voltage over I_D, smaller SCEs, higher transconductance (gm),

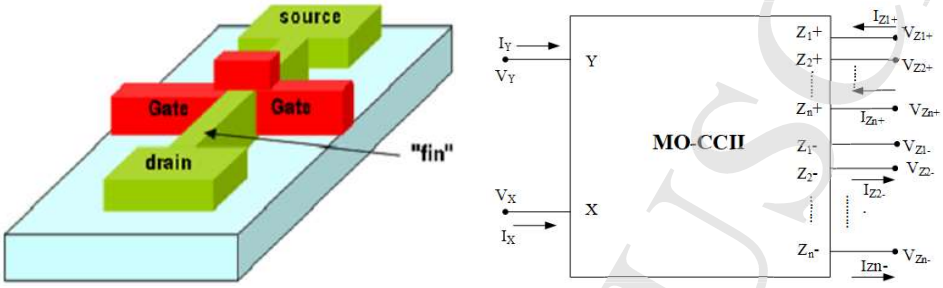


Fig. 1: (a) Basic Structure of FinFET[21] (b) Symbolic representation of MO-CCII

ideal sub-threshold voltage. Therefore, FinFETs are easier to scale down physically as well as electrically when compared with Bulk CMOS. The effective width of the transistor is calculated using Eq. (1)

$$W_{eff} = n * (2 * H_{FIN} + T_{FIN}) \tag{1}$$

where n is the number of fins, H_{FIN} is fin-height and T_{FIN} is fin thickness. For 20nm PTM model of FinFET, T_{FIN} is 15nm and H_{FIN} is 28nm. FinFETs provide a road-map to scale down the feature size up to 7nm.[17–19]

A further advantage of the multi-sided gate is more drive current per unit area than Bulk CMOS−the height of the fin can be utilized to make a channel with a bigger effective volume than a planar device with a similar equivalent gate length. This converts into better effective performance. The additional performance capability of FinFETs can be utilized to accomplish higher frequency compared with a planar device for a given power budget.[20]

3. Current Conveyor Overview

CCII has four ports namely X, Y, Z+ and Z− ports. X and Y ports are input ports and Z+ and Z− are output ports. It has a high input impedance port for voltage inputs, one low input impedance port for current input, and two high output impedance ports for current outputs.

CCII is a current mode device which delivers the current from input X port to the output Z+ and Z− ports with unity gain and voltage from Y port to X port with unity gain. CCII provides better high frequency response when compared with OPAMP. Therefore CCII has an edge over OPAMP for high-frequency applications. Because of its versatility, CCII is suitable for both VM as well as CM circuits. CCII has been used to implement precision rectifiers, capacitance multipliers, impedance converters, integrators, differentiators, filters, *etc.*[22–29] The symbol and transistor level diagram are shown in Fig. 1b and Fig. 2 respectively. The characteristic equa-

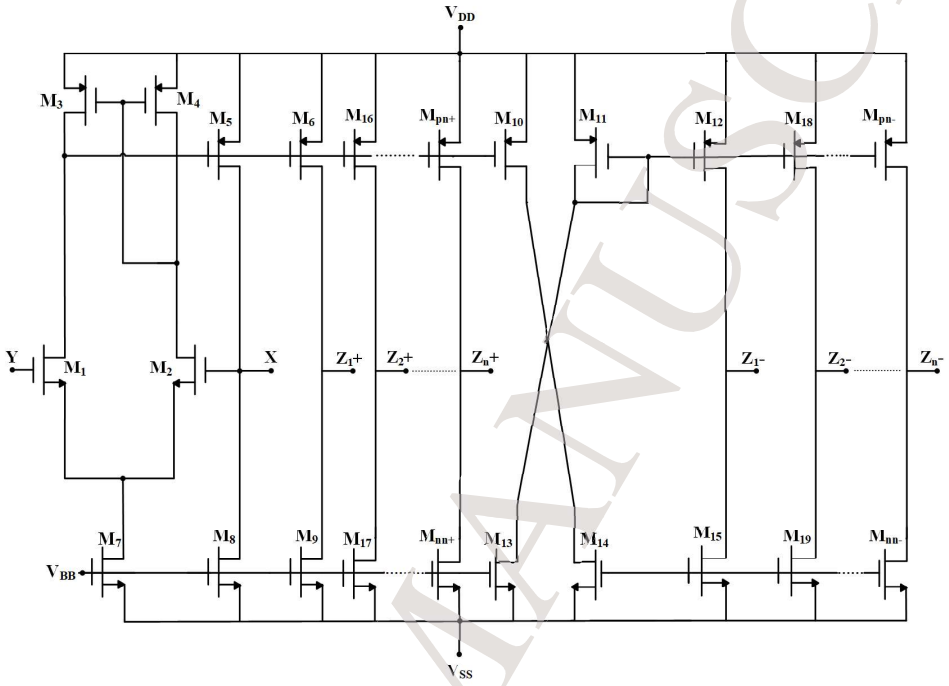


Fig. 2: Transistor Level Realization of MO-CCII

Table 1: PARAMETERS OF FinFET BASED MO-CCII (L=100nm for all transistors)

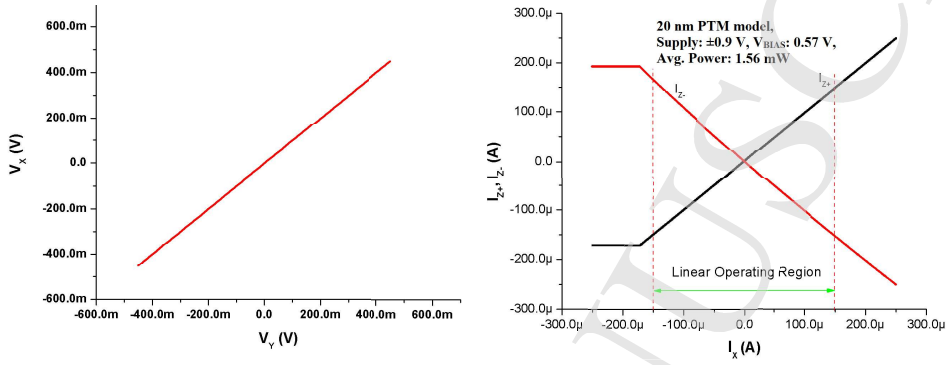
Transistors	M_1, M_2	M_3, M_4	M_5, M_6, M_{10}	M_{16}	M_7	M_8, M_9	M_{13}, M_{17}
No of Fins	2	4	45	5	60	10	8

tion for CCII can be represented as follows.

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z\pm} \end{bmatrix} \tag{2}$$

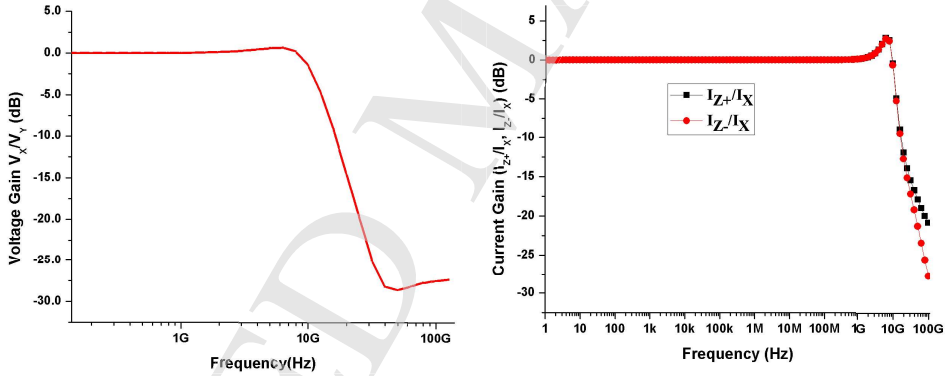
where V_X and V_Y are the input voltages at X and Y ports respectively, I_Y, and I_X are input currents at Y and X ports and $I_{Z\pm}$ are the output currents at Z± ports, and $V_{Z\pm}$ are the voltages at Z± ports. Ideal CCII must have following properties.

(a) Infinite input impedance (Z_Y) at Y port for voltage inputs. (b) Zero input impedance (Z_X) at X port for current inputs. (c) Infinite output impedances ($Z_{Z\pm}$) at $Z\pm$ ports for current outputs. (d) Infinite BW. (e) Unity Voltage transfer gain between Y and X ports. (f) Unity Current transfer gains among X and $Z\pm$ ports.



(a) (b)

Fig. 3: (a) Voltage Transfer Characteristics between Y and X ports (b) Current Transfer Characteristics among the X, Z+ and Z− ports

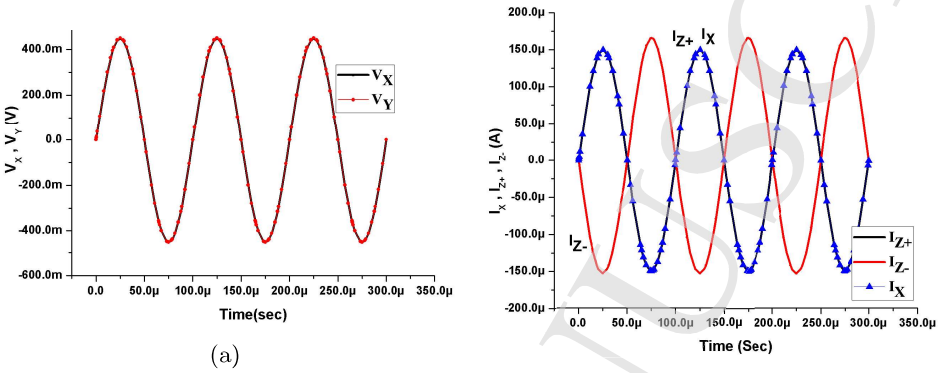


(a) (b)

Fig. 4: (a) Frequency Response of Voltage Gain (V_X/V_Y) (b) Frequency Response of I_{Z+} and I_{Z-}

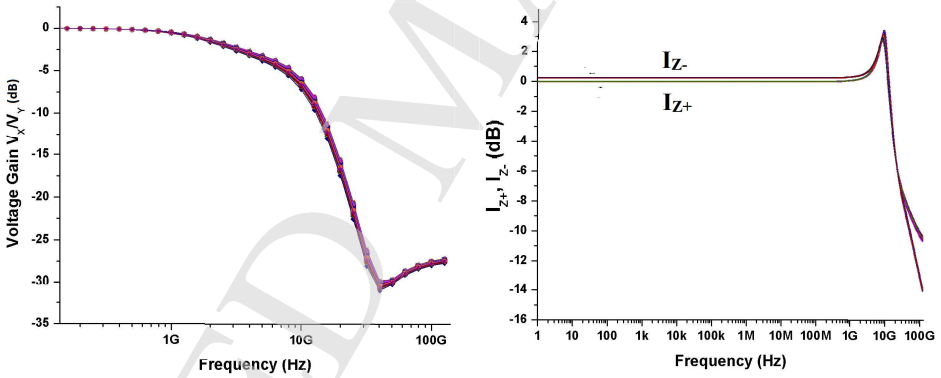
4. Performance Investigation of FinFET based MO-CCII

With the advent of FinFET, researchers made important analog as well as digital circuits[19] like OTAs and OPAMPs,[30,31] SRAMs,[32,33] ring oscillators,[34] Schmitt trigger,[35] *etc.* using these devices. But as far as author's knowledge, FinFET based architecture of CCII was first proposed in.[36] In this paper, an MO-CCII using 20nm FinFET has been designed and its performance is investigated using HSPICE. To ensure better cascading, input impedance for voltage input Y port must be very high, input impedance for current input X port must be very low and output



(a) (b)

Fig. 5: (a) Transient Response of Voltage Follower between Y and X ports (b) Transient Response of Current Relationship among the X, Z+, and Z− ports



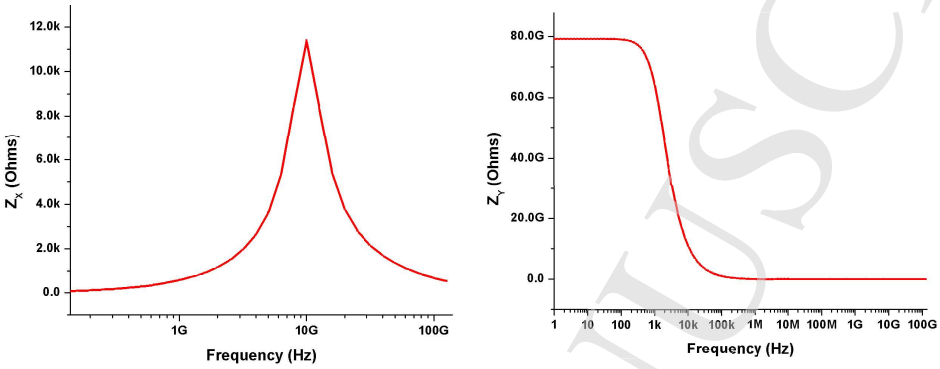
(a) (b)

Fig. 6: (a) Monte Carlo analysis for Voltage Gain (V_X/V_Y) (b) Monte Carlo analysis for I_{Z+} and I_{Z-} using 2000 samples

impedance for current output Z± ports must be very high.

All simulations are done using HSPICE. FinFETs used in this paper are based on 20nm PTM models. Power supply voltages used are $\pm 0.9V$ and biasing voltage used is 0.57V, for the proper operation of CCII. Average power dissipation is 1.56mW. The parameters of various transistors in the designed module are given in Table 1.

The DC characteristics of CCII are shown in Fig. 3. DC voltage transfer characteristics between ports Y and X are shown in Fig. 3a. A DC voltage is applied at Y terminal and the voltage at X terminal follows it linearly according to the char-



(a) (b)

Fig. 7: (a) Frequency Response of Port X Impedance (b) Frequency Response of Port Y Impedance

acteristic equation of CCII. The graph between V_Y and V_X shows linear behavior from $-450mV$ to $450mV$.Fig. 3b shows the current transfer characteristics among X, Z+ and Z− ports. A DC current is applied at X terminal of the CCII and shows good linear behavior among X, Z+, and Z− ports and shows linear behavior from $-150\mu A$ to $150\mu A$.

AC characteristics of CCII are shown in Fig. 4. Fig. 4a shows the AC voltage transfer characteristics between V_X and V_Y. The 3dB BW of voltage transfer gain is 11.2GHz. Fig. 4b shows the AC current transfer characteristics. The 3dB BW obtained for current transfer gain is 11GHz.

Results of transient analysis of CCII are presented in Fig. 5. Fig. 5a shows the transient response of voltage follower action of the ports Y and X. It clearly shows that port X voltage follows the voltage at port Y. Fig. 5b shows the transient response of current transfer characteristics among port X and ports Z+ and Z−.

Monte Carlo analysis has been done on performance parameters (Voltage Gain and Current Gain). The independent parameter of H_{FIN} has been chosen and assumed to have independent Gaussian distribution with 3σ variation of 10% with 2000 samples.[37] H_{FIN} has been taken because it has a major contribution to the effective width of fin of the transistor as given in (1). Monte Carlo analysis for voltage as well as current gain are shown in Fig. 6.

The port impedances of the device are shown in Fig. 7. Fig. 7a shows the frequency response of port X impedance. Z_X has a value of $1.5K\Omega$ for a frequency of 2.5GHz. Ideally, the value of Z_X must be very low and the simulated results are also providing the quite low value of Z_X. Fig. 7b shows the frequency response of port Y impedance. For lower frequencies, Z_Y is $79G\Omega$ and has a value of $377K\Omega$ for a frequency of 2.5GHz. Ideally, port Y impedance must be very high and the simulated results are also providing the quite high value of Z_Y.

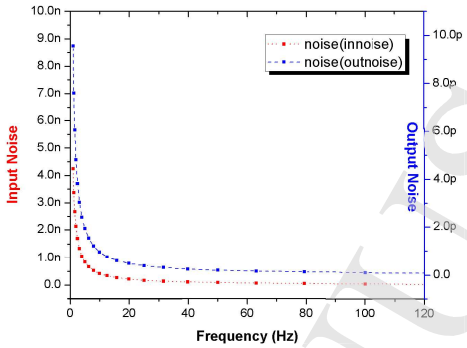


Fig. 8: Noise Analysis of DO-CCII with V_Y as input port

Total output noise is $9.56pV/\sqrt{Hz}$ and equivalent input noise at V_Y is $4.24nV/\sqrt{Hz}$ as shown in Fig. 8. Also, Table 3 shows the comparison of noise performance of the proposed MO-CCII with other state-of-the-art circuits. The proposed circuit can provide much better noise performance over the other circuits except.[36] This significant improvement in noise performance is attributed to the smaller T_{FIN} of FinFETs. The flicker noise and its temperature dependence become smaller as T_{FIN} becomes lower than 30 nm (In this design, it is 15 nm). This effect comes into the picture because the smaller T_{FIN} provides relaxation of the vertical electrical field from channel to gate electrode. Therefore FinFET with smaller T_{FIN} is more attractive in designing analog circuits than bulk CMOS because of its excellent noise performance.[38]

Table 2 shows the comparison of the performance of the proposed MO-CCII with other state-of-the-art circuits. The proposed circuit can provide much better performance in terms of high frequency response. The proposed MO-CCII provides a 3dB BW of 11GHz for currents while 11.2GHz voltage gain. Also, one can see from the table that the CCII in[39] provides 3dB BW of 195MHz for current gain while 377MHz for voltage gain; similarly, the CCIIs in,[40],[41],[42] and[43] also providing 3dB BW for current as well as voltage gains in MHz range only.

5. Multi-Function Bi-quadratic Filter based on FinFET based MO-CCII

A VM multi-function bi-quadratic filter based on proposed MO-CCII which does not need any resistors employing CCII as an active building block is proposed. Fig. 9a shows the circuit proposed in[47] and Fig. 9b shows the implementation of Fig. 9a using voltage controlled resistor by making use of a single transistor in linear region as a variable resistor to control filter properties electronically. Two CCIIs, two capacitors and two FinFETs working in the linear region are utilized to realize bi-quadratic BP, LP, and HP transfer functions (TFs) all together with a similar

Table 2: Performance Comparison of the Proposed MO-CCII with State-of-the-Art Circuits

Performance Parameters	Proposed MO-CCII	[39]	[40]	[41]	[42]	[43]
Process	**20nm FinFET**	0.18m	0.13m	0.18m	0.5m	0.35m
Technology	**FinFET**	CMOS	CMOS	CMOS	CMOS	CMOS
Supply Voltage (V)	**±0.9**	±0.9	1.5	**±0.5**	**±0.75**	±1.65
Power Dissipation (mW)	**1.56**	0.45	1.5	120	1.62	1.3
DC Current Range (A)	**±150**	±80	±20	**±24000**	±100	±3000
DC Voltage Range Y (mV)	**±450**	±350	Rail to Rail	±240	–	−1.43 to +1.1
3dB BW for I_{Z+}, I_{Z-}	**11GHz**	195MHz	99MHz	**30.2MHz**	100MHz	915MHz
3dB BW for V_X/V_Y	**11.2GHz**	377MHz	94MHz	**36MHz**	–	810MHz

Table 3: Noise Performance Comparison of the Proposed MO-CCII with State-of-the-Art Circuits

Noise Performance Parameters	Proposed MO-CCII	[44]	[45]	[46]	[42]	[36]
Output Noise	**9.56 pV/$\sqrt{Hz}$**	4.51 nV/$\sqrt{Hz}$	23 nV/$\sqrt{Hz}$	0.5 μV/$\sqrt{Hz}$	4.1 nV/$\sqrt{Hz}$	9.56 pV/$\sqrt{Hz}$

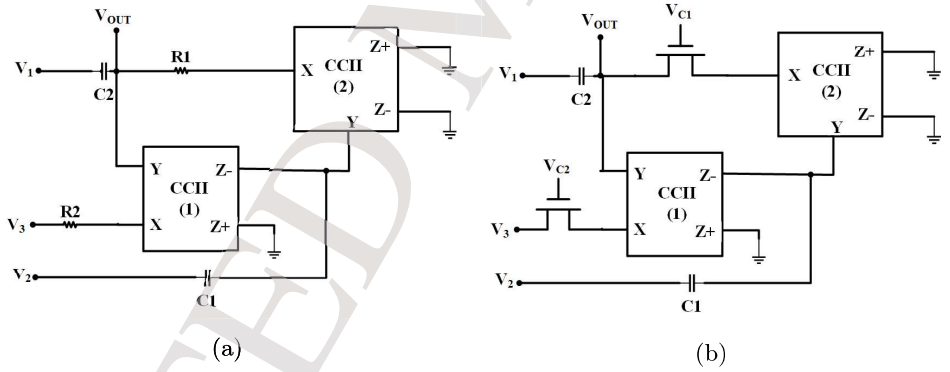


Fig. 9: (a) Block Diagram of Filter reported in[47] (b) MO-CCII based Multi-Function Filter Implementation of Fig. 9a using voltage controlled resistor

arrangement. The proposed VM multi-function filter utilizes two floating capacitors which can be effectively realized in these days' IC technology.[48]

The transfer function for the proposed circuit can be obtained using direct analysis and can be expressed as follows.

$$V_0 = \frac{s^2 R_1 R_2 C_1 C_2 V_1 + s R_2 C_1 V_2 + V_3}{s^2 R_1 R_2 C_1 C_2 + s R_2 C_1 + 1} \tag{3}$$

Table 4: Performance Characteristics of the proposed filter

Performance Factor	Supply Voltage V_{DD} (V)	Total Power Dissipation (mW)	Frequency of operation (GHz)	Bandwidth (MHz)
GHz frequency range	±0.9	3.26	2.1	720

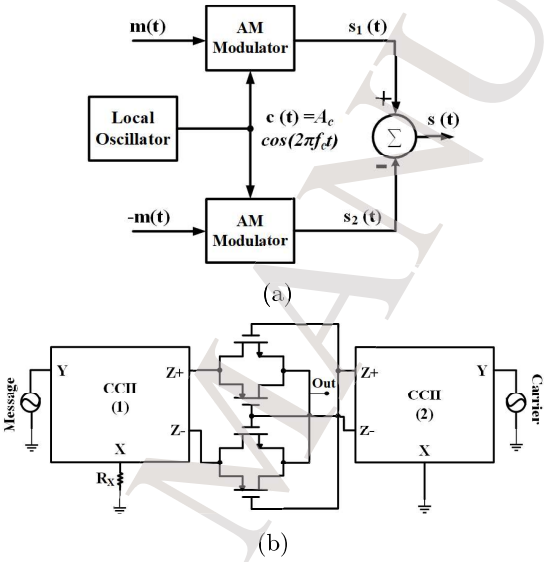


Fig. 10: (a) Block Diagram of a Balanced Modulator (b) MO-CCII Based Balanced Modulator Implementation of Fig. 10a

The three TFs obtained using (3) are: (a) Second-order low-pass filter can be obtained using $V_1 = V_2 = 0$ (grounded), (b) Second-order band-pass filter can be obtained using $V_1 = V_3 = 0$ (grounded), and (c) Second-order high-pass filter can be obtained using $V_2 = V_3 = 0$ (grounded). Therefore the natural frequency (ω_0) and quality factor Q can be given as:

$$\omega_0 = \frac{1}{(R_1 R_2 C_1 C_2)^{1/2}} \; and \; Q = (\frac{R_1 C_2}{R_2 C_1})^{1/2} \tag{4}$$

Fig. 11a shows the filter responses for the proposed filter. Component values taken are $C_1 = 0.005$pF and $C_2 = 0.05$pF. The frequency of operation obtained for the filter is 2.1GHz. The total power consumed by the multi-function filter is 3.26mW. Table 4 shows the performance characteristics of the proposed filter in GHz frequency range.

Table 5: Performance Characteristics of the proposed balanced modulator

Performance Factor	Supply Voltage V_{DD} (V)	Average Power Dissipation (mW)	THD	Message Signal Frequency (MHz)	Carrier Frequency (GHz)
GHz frequency range	±0.9	2.97	4.41%	50	1

6. Balanced Modulator

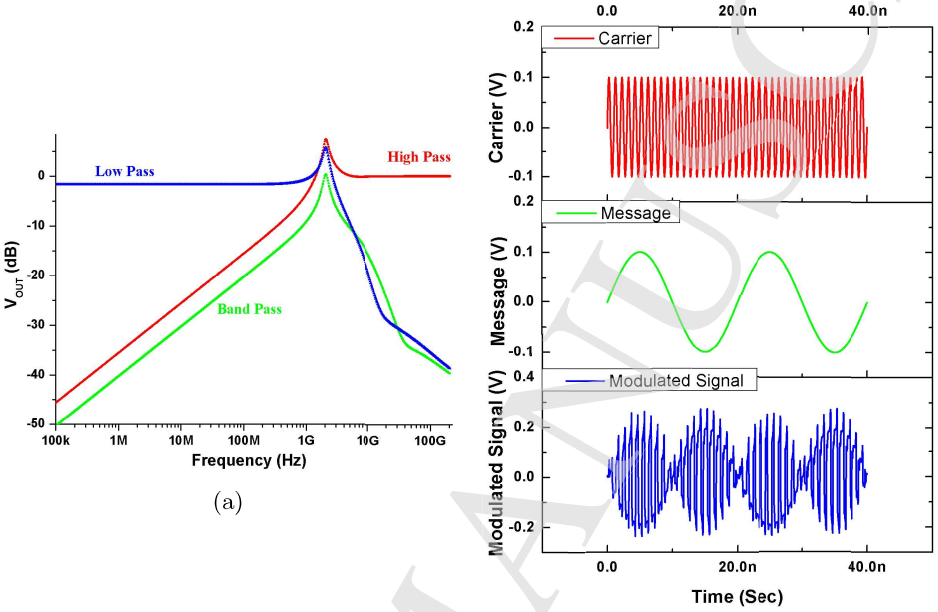
A Balanced Modulator might be characterized as a circuit in which two non-linear devices are associated in a balance mode to deliver a Double Sideband Suppressed Carrier (DSBSC) signal. The balanced modulators are utilized to suppress the undesirable carrier in an AM wave. The carrier and modulating signals are connected to the inputs of the balanced modulator and the DSB signal with the suppressed carrier can be obtained at the output of the balanced modulator. In this manner, the output comprises the upper and lower sidebands only. The general block diagram of a balanced modulator is shown in Fig. 10a and its MO-CCII implementation is shown in Fig. 10b.[49]

The simulation results for the proposed balanced modulator are shown in Fig. 11b. The message signal has a frequency of 50MHz and the carrier frequency is 1GHz. The Total Harmonic Distortion (THD) in the output comes out to be 4.41%. The average power consumed by the balanced modulator is 2.97mW. Table 5 comprises of the balanced modulator's performance characteristics for its application in GHz frequency range.

Although, the values of Z_{Y1} and Z_{Y2} are quite high at 1GHz but they are not infinite. Therefore, the output performance of the proposed balanced modulator operating at 1GHz gets affected and the THD becomes 4.41% otherwise it will remain much lower than this value.

7. Conclusion

In this paper, the performance analysis of 20nm FinFET based MO-CCII has been done using HSPICE. DC as well as AC analysis shows great coherence between the theoretical and simulated behavior of the device. The DC voltage range for the proposed CCII is $-450mV$ to $450mV$ and AC analysis shows 3dB BW of currents and voltage gains as 11GHz and 11.2GHz respectively. The port impedances of the device also show nearly ideal values. Simulation results show that FinFET based approach has an edge over CMOS based approach beyond 22nm channel length. Also, a VM multi-function bi-quadratic filter capable of simultaneous realization of LP, BP and HP TFs from the same circuit topology is proposed. It depends on two CCIIs, two floating capacitors which can be easily realized in these days' IC process and two FinFETs working as a variable resistor. The proposed balanced modulator works perfectly in GHz frequency range. It utilized proposed FinFET based CCIIs and FinFETs only. It is expected that the proposed circuits will be valuable in numerous fields, for example, signal processing, control engineering, and



(a)

(b)

Fig. 11: (a) Filter Responses of Multi-function Bi-quadratic filter using MO-CCII (LP response shown in blue, BP response shown in green, and HP response shown in red) (b) Results for the proposed balanced modulator (DSBSC modulated signal shown in blue, message signal with 50MHz frequency shown in green, and carrier signal with 1GHz frequency shown in red

broadcast communications.

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