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Tunable Memristor Emulator using Off-The-Shelf components

Vipin Kumar Sharma[a]*, Mohd. Samar Ansari[a,b], T. Parveen[a]

[a]*Z.H. College of Engineering and Technology, Department of Electronics Engineering, Aligarh Muslim University, Aligarh, India*
[b]*Software Research Institute, Athlone Institute of Technology, Ireland*

Abstract

Emerging memristor technology is as of late drawing broad consideration due to its potential for several applications. But, the non-availability of solid-state memristive devices puts a practical limitation. So, this paper proposed the concept and design of a practical memristor emulator, which can be used to imitate the behaviour of the well-known ideal memristor model developed by the HP Lab. This circuit contains off-the-shelf components such as AD844, AD633, voltage variable resistor (VVR) and few passive components. This circuit provides voltage tunability, an additional advantage over current tunability, which requires a complex circuitry. All the fingerprints of nano-scale memristor behavior are validated by the derived mathematical relations and simulation verification. Further, the robustness of the circuit has been demonstrated for statistical (10% deviation in passive components) and environmental variations (10% deviation in supply voltages). Also, the proposed circuit has been tested for a wide temperature range. Eventually, the proposed circuit is compared with the previously published emulators to illustrate the advantages of the proposed design.

Keywords: Memristor Emulator; Emerging Technology; Voltage Variable Resistor (VVR), Non-linear Circuit Element, Voltage Tunability

Corresponding author. Tel.: +91 8445184074

E-mail address: aligvipin@gmail.com

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1. Introduction

As per recent trends, CMOS integrated circuit technology progressively moving towards saturation mainly in terms of scalability. Now the researchers are trying to explore viable technologies that have potential to replace the conventional CMOS technology. So, the emerging technologies beyond CMOS such as memristor proved to be a promising candidate due to its nano-scale size and low power applications.

In 1971, L.O. Chua firstly reported the existence of *missing element* "Memristor" by mathematically establishing the *Charge-Flux* relationship. The memristor abbreviated as *Memory-Resistor,* considered as a fourth basic circuit element in addition to Resistor, Capacitor and Inductor [1]. Likewise, the other three circuit element, memristor is a two-terminal element but its peculiar characteristics like nonlinear characteristic, non-volatility and high density storage technology [12] makes it different from others. Also, Memristor has a tendency to hold the resistance state until or unless if no change in magnitude and polarity of the excitation (Voltage/Current). This makes memristor a standard non-volatile memory element, which has an extensive impact on informatics and neuromorphic processing [13-16].

Due to complexity in fabrication, further research on memristor became stagnant for few decades. But, in 2008, after successful fabrication of Titanium di-oxide (TiO_2) memristor by HP laboratory opens up the new era of possibilities [2]. From that point forward, different sorts of memristors have been created with various materials, for example, the ferroelectric memristor [3], the tantalum oxide memristor [4, 5], and the spintronic memristor [6]. Be that as it may, because of their natural intricacy, these later discovered memristors can scarcely be mathematically characterized. Consequently, the utilization of the HP TiO_2 memristor stays famous. However, the design of the memristor by HP laboratories is still not available on the commercial market due to its manufacturing complexity and high costs, which delay the commercialization memristor's real-time applications. So, different approaches to mimic the actual physical device have been proposed.

In perspective on the relationship between charge and flux, researchers proposed to utilize nonlinear functions to mimic a memristor and examine a memristor circuit quantitatively. Chua pointed out that the monotonous and piecewise linear nonlinearity can characterize a memristor [7]. Bao et al. suggested use of quadratic and cubic non-linear functions to describe a memristor, and accomplished a further study of chaos and bifurcation by replacing their models into Chua's circuit [8–11]. The development of mathematical models yielded some progress in the study of transient as well as dynamic behavior of memristor circuits.

To further investigate the properties of memristor circuits, an assortment of memristor emulators have been created, including the HP TiO_2 emulator [17], the quadratic flux-controlled emulator, the cubic flux-controlled emulator [8,9–11,18], and the integrator based SPICE emulators [19]. With the assistance of these emulators, it is discovered that a few circuits containing diode-bridge [20] and light-dependent resistors [21] show memristor attributes under specific structures. Furthermore, a variety of memory elements based analog circuits have been developed which follows the conventional definition of memristor [22-25, 41].

In this paper, a simplified memristor emulator circuit using Off-The-Shelf components has been proposed. This circuit uses a voltage variable resistor using two PMOS which provides on-chip voltage tunability. The circuit realized follows all the three signature characteristics of memristor device such as Current-Voltage characteristic should have a (1) Hysteresis curve (2) curve should be pinched (3) Non-linear Hysteresis curve becomes linear for higher frequencies. The functional verification of the proposed circuit has been done using mathematical relationship as well as simulation results.

2. Mathematical Modeling of Memristor

The nano-scale structure of TiO_2 based Memristor as shown in Fig. 1 has the typical dimension of the order of 10nm [2]. This structure consists of two regions namely doped and un-doped having different conductivities. Depending upon the position of the boundary between two regions this device has many resistance levels possible. Pt electrodes at each side of structure are used for electrical connections.

According to HP's linear model of the TiO_2 based structure of Memristor [2], the relationship between voltage and current can be expressed as (1):

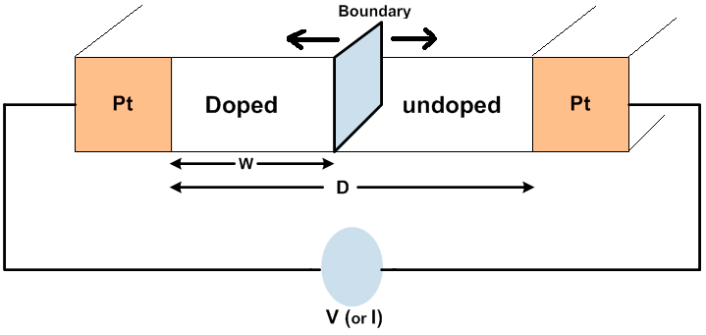

Fig. 1. Nano-scale structure of HP's TiO_2 Memristor [2]

$$v(t) = \left[R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right] i(t) \tag{1}$$

Where, D is the total width of the linear structure of the Memristor *i.e.* the sum of width of unionized (un-doped) and ionized (doped) region. w is the length of ionized region which defines the position of the boundary. The R_{off} and R_{on} are the low and high state resistance of the device when w is equal to zero and D respectively. The value of w at any time depends on the cumulative value of current at that instant as shown in Eq. (2);
The rate of movement of the boundary between two regions can be defined as:

$$\frac{\partial w(t)}{\partial t} = \mu_v \frac{R_{on}}{D} i(t) \tag{2}$$

Where, μ_v is the average ion mobility. Using Eq. (1), (2) and with assumption $R_{OFF} \gg R_{ON}$, the expression of Memristance can be simplified as

$$M(q(t)) = R_{off}\left(1 - \mu_v \frac{R_{on}}{D^2} q(t)\right) \tag{3}$$

The above Eq.(3) is a generalized expression for charge dependent memristance and used as the reference for the designing of memristor emulators. This expression is modeled in Biolek's ideal model of memristor for circuit applications with the model parameters: R_{on}=100, R_{OFF}=10K, μ_v= 10f and D=10n [26]. Fig. 2 shows the current-voltage relationship of pinched hysteresis nature for the given model parameters.

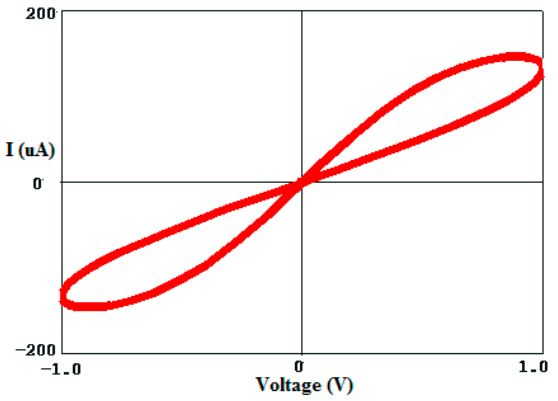

Fig. 2. Current-Voltage characteristic for SPICE model of memristor [26]

Table 1. Comparison of the proposed work with similar existing work

Ref.	No. of passive Components (Floating)	No. of active Components	No. of passive Components (Grounded)	Technology	Power Supply (V)	Tunability mode
[28]	3R	4 CCII, 2 Diodes	1R, 4C	BJT	± 10	X
[29]	1R	4 CCII, 1 Multiplier, 1 op-amp	7R, 1C	BJT	± 15	X
[30]	1R	10 MOS, 2 op-amp, 1 multiplier	1R, 1C	CMOS	± 5	X
[31]	2R	12 OTA, 1 multiplier	2R, 1C	BJT	± 10	current
[32]	1R	6 OTA, 1 multiplier	1R, 1C	BJT	± 10	current
[33]	2R,1D	3 CFOA	2R, 2C	BJT	-	X
[34]	-	2 CFOA, 1 OTA	3R, 2C	BJT	± 12	current
[35]	2R	4 AD844AN, 1 multiplier	3R, 1C	BJT	± 10	X
[36]	3R	4 CCII, 3 OTA	3R, 1C	BJT	± 15	current
[37]	1R	2 AD844AN, 1 multiplier	1R, 1C	BJT	± 10	X
[38]	1R	1 CCII, 1 multiplier	1C	BJT	± 10	X
[39]	3R, 1D	2 AD844AN, 1 op-amp	2R, 1C	BJT	± 10	X
[40]	3R	3 AD844AN, 1 multiplier	2R, 1C	BJT	± 10	X
Proposed work	**2 R**	**2 AD844AN, 1 Multiplier, 2 PMOS**	**1R, 1C**	**BJT & CMOS**	**± 10**	**voltage**

3. Circuit Description

The circuit as shown in Figure 3, basically contains 3 AD844 ICs, a Multiplier IC (AD-633), one VVR along with few resistors and capacitors. Basically, this design of memristor emulator is based on charge controlled approach *i.e.* memristance should be a function of charge which is described below as:
The current conveyed from X to Z terminal of AD844 (1) and AD844 (2) is

$$I_{Z1}(=I_{X1}) = I_{Z2}(=I_{X2}) = \frac{I_{in}}{2} \qquad \text{(Since, } R_1=R_2=R\text{)} \tag{4}$$

The voltage developed across VVR and capacitor appears on voltage output terminals of AD844 (1) and AD844 (2) respectively as

$$V_{W1} = \frac{I_{in}}{2}R_v \ , V_{W2} = \frac{1}{2C} * \int I_{in} \tag{5}$$

where, R_v & C is the resistance and capacitance of VVR and capacitor respectively.
The voltage obtained at the output of multiplier (AD633) is

$$V_{Wm} = V_{W1}.V_{W2} = \frac{I_{in}}{4C}R_v * \int I_{in} \tag{6}$$

While on solving VVR [27], $$R_v = \frac{1}{2\mu_p C_{ox}\frac{W}{L}(V_c - V_t)} \tag{7}$$

The output of multiplier which is feedback to the Y-terminals of both AD844 (1) and AD844 (2) is then transferred to X-terminals, so on equating the currents

$$\frac{I_{in}}{2} = \frac{V_{in} - V_{Wm}}{R} \tag{8}$$

On solving equation Eq. (6) & (8), we get the expression for memristance as

$$M(\int I_{in}) = \frac{V_{in}}{I_{in}} = \frac{R}{2} + \frac{R_v}{4C} * \int I_{in} \tag{9}$$

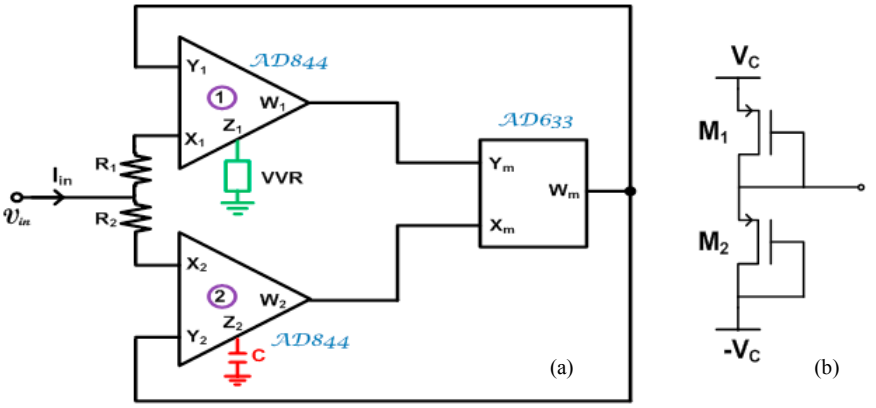

Fig. 3. (a) Circuit implementation of Memristor Emulator (b) VVR [27]

The above expression is identical to the basic definition of charge controlled memristance as given in Eq. (3). The Eq. (9) contains two terms: Linear Time-variant and Linear Time-invariant. The time-variant and time-invariant terms decides the area and the slope of Hysteresis curve respectively. Also, time-variant term includes voltage controlled resistance, R_v which is given in Eq. (7) , incorporates the tunability feature in terms of area of the curve or the memristance variation. Further, in order to understand the effect of frequency on the hysteresis curve of memristor, consider an input signal $V_m \sin\omega t$ and corresponding relationship can be obtained as

$$M(\omega) = \frac{V_{in}}{I_{in}} = \frac{R}{2} + \frac{V_m R_v}{2wRC} * \cos(\omega t - \pi) \quad (10)$$

Where, $M(\omega)$ represents the memristance in frequency domain. The above expression shows inverse relationship of memristance with frequency which is one of the signature characteristics of memristor.

4. Results and Discussion

The proposed memristor emulator is shown in Figure 3. The circuit employs off-the-shelf components; AD-844's, AD-633, two PMOS transistors and some passive components. The PMOS transistors are used for designing the VVR, which facilitate the emulator circuit with voltage controllability. To test the circuit workability, PSPICE simulation has been done. The components values considered for the simulation are: R_1 & R_2 is equal to 5 KΩ and C is chosen according to the range of operating frequency. The PMOS transistors used in the circuit is TSMC 0.25µm process and having the aspect ratio (W/L) for both PMOS is 5µm/0.25µm. The supply voltages used are ±10V.

Now, the functional verification of the proposed memristor has been done using sinusoidal voltage excitation $V_{in} = V_m sin2\pi f$t where, V_m & f is the amplitude and frequency of input signal. For this work, the amplitude of 2 volts has been taken while frequency is different for each case. Fig. 4 shows the Hysteresis characteristic for proposed memristor emulator at 100 Hz and 1 KHz frequency. It can be observed from figure that each plot shows the three basic fingerprints of memristor. Fig. 5 presents the current and voltage waveforms *w.r.t.* time. This figure confirms the non-linear nature of the proposed emulator circuit. Now, in order to understand the effect of varying the capacitance value at fixed frequency, Hysteresis characteristics have been shown for capacitance of 100n, 200n and 300nF in Fig. 6. It can be noted from this figure that on increasing the value of capacitance, the area of hysteresis loop decreases. This effect is also mathematically validated by Eq. (9), that on increasing the value of capacitance, the time-variant term decrease hence the area of hysteresis loop decreases. Thereafter, the tunability feature of the proposed circuit has been shown in Fig. 7. In this figure, Hysteresis loop and the memristance value for the change in voltage from 0.5 to 2V has been presented. The mathematical justification for the above is given in Eq. (9), as the change in control voltage changes the resistance of VVR which alters the time-variant term of Eq. (9). Hence, the area of loop as well as memristance has been changed.

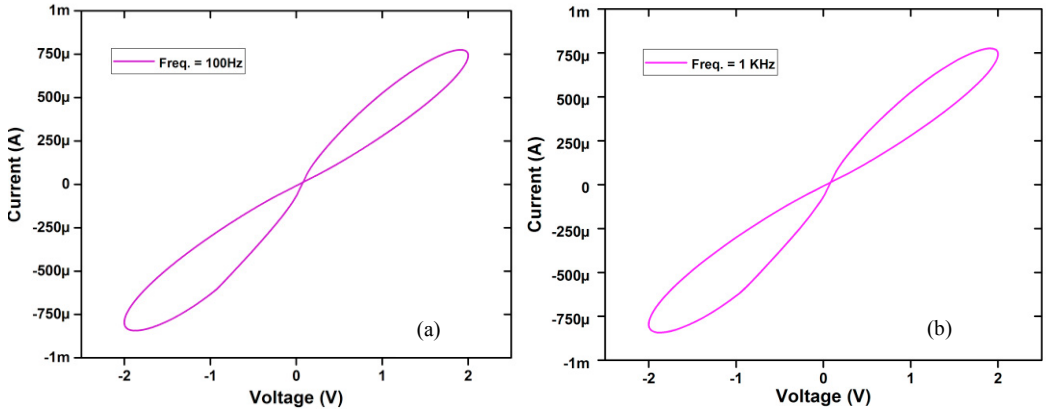

Fig. 4. Hysteresis Characteristics Plot for the proposed memristor emulator (a) 100 Hz (b) 1 KHz

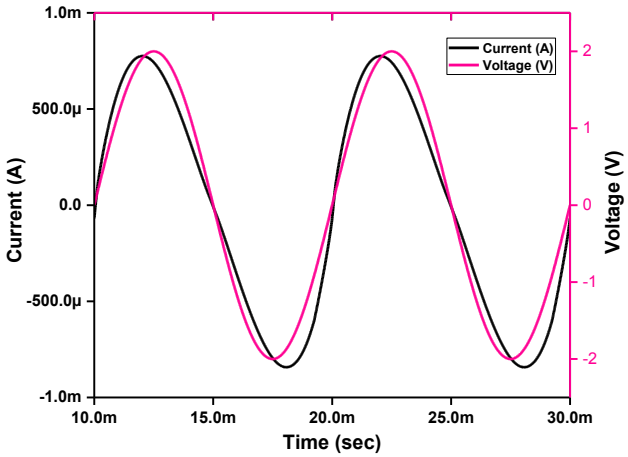

Fig. 5. Voltage (excitation) and Current (response) waveform at 100 Hz frequency

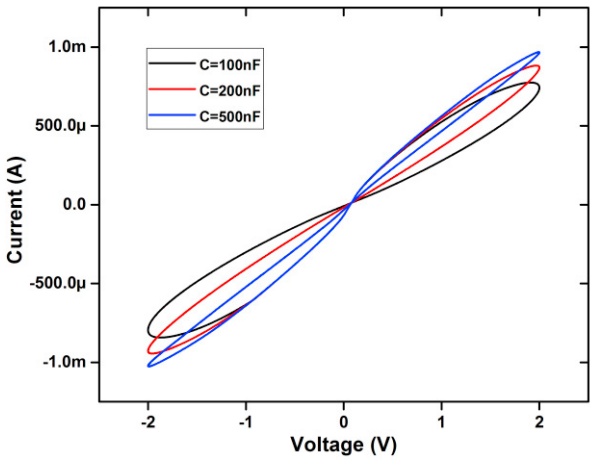

Fig. 6. Hysteresis Characteristics Plot of the proposed memristor emulator for different capacitance values

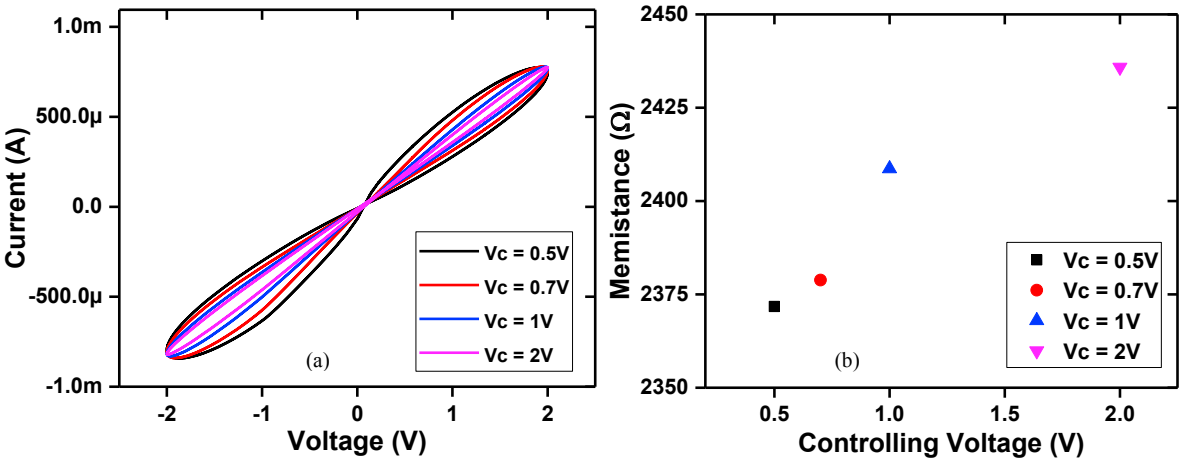

Fig. 7. Tunability feature for proposed circuit (a) Hysteresis Characteristics for different values of controlling voltage (b) Memristance values

Furthermore, in order to test the reliability of the proposed circuit, the impact of statistical and environmental variations on the performance of the circuit has been considered. The performance matrices such as signature characteristics of memristor and memristance value are investigated. Now, the statistical variation which is estimated by the Monte-Carlo simulation with Gaussian distribution of ±10 % (3 σ) deviation in all the passive components is shown in Fig. 8. In Fig. 8(a), it can be observed that all the samples follow the signatures characteristics and Fig. 8(b) shows the Histogram plot having a mean value of memristance as 2347.57 Ω and sigma equals to 170.64 Ω.

Next, the effect of environmental variations such as supply voltage (V_{DD} or V_{SS}) and temperature has been observed. Fig. 9 shows the dependence of signature characteristics and memristance value on the supply voltage (V_{DD} or V_{SS}) with ±10 % deviation in nominal value. It can be seen that the memristance changes by -3.6% and -4.5% for +10% and − 10% variation in supply voltages respectively. Also, despite of slight variation in Hysteresis loop, the signature characteristics didn't altered. Likewise, the thermal reliance of memristor emulator signature characteristics has been shown in Fig. 10. It is observed from the figure that the Hysteresis curves obeys the signature characteristics for a wide temperature range (-27°C to 100°C).

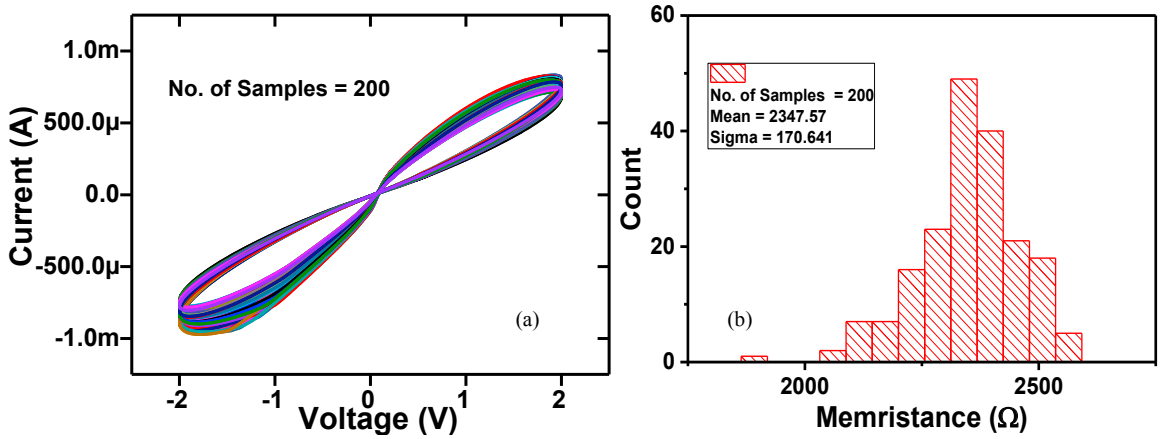

Fig. 8. Results of Monte-Carlo simulation (a) Hysteresis characteristics plot (b) Histogram plot for memristance

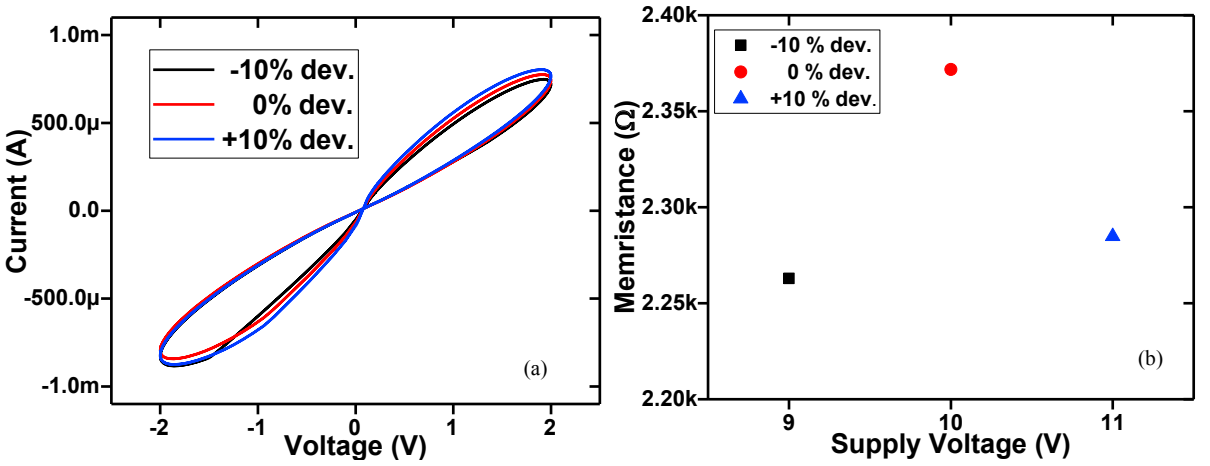

Fig. 9. Results showing effect of 10% deviation in supply voltage (a) Hysteresis characteristics (b) Memristance values

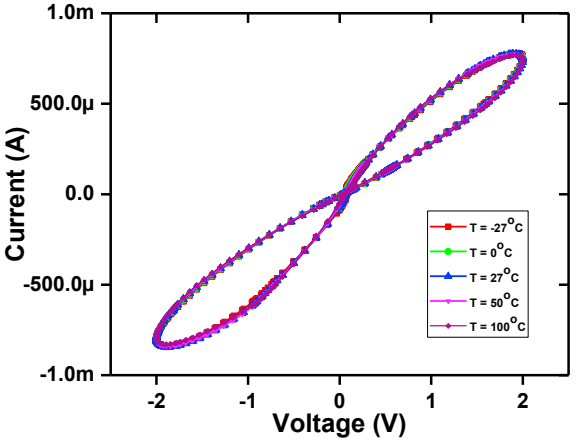

Fig. 10. Hysteresis characteristics plot for variation in temperature (-27℃ to 100℃)

5. Conclusion

In this work, the memristor emulator circuit using off-the-shelf components has been proposed. This circuit can mimic the TiO_2 mathematical model given by HP labs. All the fingerprints of nano-scale memristor behavior are validated by the derived mathematical relations as well as simulation verification. Also, the reliability of the proposed circuit has been tested for statistical variation in all the passive components and environmental variations (Supply voltages and Temperature). The results obtained show the satisfactory performance for the deviation in passive and supply voltages for a wide temperature range. This circuit fulfils the need of actual physical device for the real world applications.

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