AEUE - International Journal of Electronics and Communications xxx (xxxx) 153575

Contents lists available at ScienceDirect

AEUE - International Journal of Electronics and

journal homepage: http://ees.elsevier.com

Regular paper

Four quadrant analog multiplier based memristor emulator using single active element

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ARTICLE INFO

Article history:
Received 10 September 2020
Accepted 6 December 2020
Available online xxx

Keywords
Memristor emulator
FQAM
CDTA
Amplitude modulation
Non-volatility

ABSTRACT

This paper presents a novel Four Quadrant Analog Multiplier (FQAM) circuit and its applications using a single active element Current Differencing Transconductance Amplifier (CDTA) and two NMOS. This circuit has a cascadability feature as it produces current and voltage outputs at high and low impedance ports, respectively. It offers additional features such as resistor-less realization, operability in voltage and trans-conductance mode, and configurable structure. Further, the FQAM circuit is configured to develop a memristor emulator based on the proposed mathematical analogy. The proposed memristor circuit contains active elements (one CDTA, two NMOS, and one Inverting Voltage buffer) and only one grounded capacitor. It offers tunability using the transconductance gain of the CDTA block. Also, the proposed memristor emulator circuit doesn't contain any additional multiplier block. The emulator circuit can be operated in both the Incremental and the Decremental mode of memristance variation. The results demonstrate the non-volatile property as well as hysteresis behavior for the wide frequency range. The effects of statistical variation in passive component, threshold voltage, and aspect ratios on the proposed circuits using Monte-Carlo simulation have been estimated. Also, the impact of non-idealities and the parasitic effects of the CDTA on the proposed circuits are investigated. In last, the capacitor-less version of the memristor emulator and its hysteresis characteristics have been demonstrated. The simulation results obtained using HSPICE, are agreed well with the theoretical analysis.

1. Introduction

Nowadays, the current research focuses on reducing the chip area along with low power consumption. So, there is a trend of realization of analog signal processing circuits using active building blocks (ABBs). Also, the use of configurable block in large architecture is favorable to reduce the complexity. The non-linear analog circuits such as Four Quadrant Analog Multiplier and Memristor are widely used analog signal processing circuits. The famous applications of the FQAM circuit are amplitude modulation, frequency doubling, modulators, sensors, neural networks, and adaptive filters. In addition, the novel non-linear applications of memristors such as chaotic circuit, multi-wing attractor, coexisting multiple attractor, hidden attractor, and hyperchaotic system have attracted the research community. Further, current conveyor circuits have received considerable attention due to their better linearity, wider bandwidth, extensive dynamic range, high slew rate, and lesser power dissipation compared with their voltage-mode counterparts, such as operational amplifiers (OAs). Also, the current mode circuits are also relevant for fabrication in CMOS technology and thus finding favor of analog circuit designers. The realization of the proposed circuits uses a versatile current mode active block CDTA (Current Differencing Transconductance Amplifier), was proposed by Biolek in 2003 [1]. Also, the CDTA chip designed and manufactured in 0.7 μm CMOS technology facilitates the realistic analog signal processing applications [2].

A multiplier circuit produces an output signal, obtained from two linear input signals with a constant designated as k. The analog multipliers can be broadly classified into two groups as voltage mode and current mode. The firstly developed FQAM was BJT based Gilbert cell and then-after several ways of implementation in CMOS technology have been reported, such as modified Gilbert cell based on variable trans-conductance technique [3] and the linear trans-conductance technique [4]. Also, the other techniques based on the operating region of MOS transistors such as voltage-controlled trans-conductance in triode region [5] and the square law characteristics in saturation region for the implementation of quarter-square identity [6] have been utilized. But, these approaches are realized for the specific purpose and are not available in commercial integrated circuit (IC) form. The recent research focused on current-mode architectures due to the ease in fabrication along-with the need of low voltage and low power for their operation. Literature contains several FQAM circuits using various active building blocks namely second generation current conveyor (CCII) [7], operational amplifers (Op-amp) [8], dual-X current conveyor (DXCCII) [9], second-generation current controlled conveyor (CCCII)[10], difer-

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https://doi.org/10.1016/j.aeue.2020.153575
1434-8411/

ential diference current conveyors (DDCC) [11], operational trans resistance amplifer (OTRA) [12], current diferencing transconductance amplifers (CDTAs) [13], current-diferencing bufered amplifers (CDBAs) [14]. However, most of these reported works on analog multipliers are having drawbacks such as an excess number of active elements [7,9,10,14] and extra active or passive elements in form of resistors [8].

Memristor, a unique two-terminal non-linear passive component, postulated by L. Chua in 1971, considered as the fourth fundamental circuit element other than Resistor, Capacitor, and Inductor [15]. Till 2008, Chua's memristor was only a concept, but soon after the physical realization and modeling of nano-scale memristor by HP labs [16], researchers have shown an interest, and then a lot of work has been started. Memristor (Memory + Resistor) is defined by the memristance (M) or memductance (W), relates the missing link between charge and flux. The memristor device also exhibits a unique pinched hysteresis characteristic between voltage and current for the periodic excitation. So, based on its peculiar properties, this device has been recently utilized in chaotic circuits based on memristive diode bridge-coupled Sallen-Key low-pass filter [17], Band-pass filter [18]. Besides non-linearity, memristor device has a distinctive property of non-volatility, makes it suitable for memory applications. But the cost and technical difficulties in fabrication of nano-scale devices have put the restriction on the commercialization of the memristor. Although, various modeling techniques have been developed to observe its behavior in electronic circuits. But, the physical verification of real-world applications requires the emulator circuits.

The literature contains a variety of active element based memristor emulator circuits with the ample of limitations and problems. The op-amp based memristor presented in [19,20] suffered in terms of linearity and operating frequency. Literature reveals that the current conveyor based memristor emulator circuits replaced the voltage-mode due to its inherited advantages. The emulator circuits [21–25] utilized basic element CCII (second generation Current Conveyor) (AD844). However, these employ different functional blocks, along with a large number of grounded and floating passive elements. Further, [26] presented a single DDCC based simplified structure. It also employs one analog multiplier and three passive elements. This work contains the simulation results for the high-frequency range (up to 1 MHz). However, it presented different structures for both modes of memristance variation (incremental or decremental). Ref.[19–26] lacks in terms of tunability, so the tunable active elements have been utilized to facilitate the electronic controlling. In [27], the complex structure has been developed using 12 OTAs (Operational Trans-conductance Amplifiers) while in [28], it uses only a single OTA. Also, both contain analog multiplier as well as floating passive elements. Further, the simpler circuit in [29] used one OTA and two MOS transistors. However, it is suitable only for a few Hz of frequencies. Moreover, [30–32] presented the multiplier-less realization of emulators using only a single type of active element OTA. However, [31,32] contains four MO-OTAs and two DO-OTAs, respectively. While [30] presented a simplified structure using single MO-OTA; however, the tunable feature is relinquished to make the multiplier-less realization possible.

The other design of memristor emulator in [33–37] also includes OTA along-with the other type of active element, to electronically control its characteristics. Ref. [36] designed a grounded and floating memristor emulator circuit with the use of OTA and the Current Differencing Buffered Amplifier (CDBA). It contains only one grounded capacitor suitable for IC fabrication. However, the incremental/decremental configuration can be achieved only after the modification in the circuit. Ref. [37] proposed an incremental/decremental floating memristor emulator containing an OTA and a Differential Voltage Current Conveyor (DVCC). It also uses a grounded capacitor, and an electronic resistor made up of two PMOS transistors. In [38], the tunable memristor emulator using two AD-844, one AD-633, and one grounded capacitor is reported. It utilized a voltage variable resistor using two PMOS for electronic controllability. However, this circuit is suitable only for lower operating frequencies.

Further, the other tunable active elements with a good frequency response are utilized in [39–41]. The emulator structures realized in [39] uses a Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA). This circuit can be operated in incremental/decremental modes for the wide range of operating frequencies (up to 1 MHz). Despite the above features, it contain three grounded and one floating passive elements, makes the design not suitable for IC implementation. The [40] presented the Current Backward Transconductance Amplifier (CBTA) based memristor emulator utilizing additional analog multiplier and few passive components (Floating + Grounded). This work requires separate circuits for two modes of memristance variation (incremental/decremental). Another memristor emulator circuit in [41] employs one CCDDCC (Current Controlled Differential Difference Current Conveyor), two passive elements (1 resistor, 1 Capacitor), and one AD-633 as an analog multiplier. This circuit provides the variation in memristance values using the current controlled intrinsic resistance of the active block. Further, the other class of memristor emulator circuits designed specifically for the chaotic circuit have been proposed. The op-amps and analog multipliers based emulator circuits in [42,20] are utilized in op-amp based active BPF filter and Wein's bridge oscillator, respectively. The memristive diode bridge emulators in [17,18] have been utilized in Sallen-Key low-pass filter and Band-pass filter, respectively. However, these chaotic circuits contains the large number of Op-Amps and multipliers which makes the design bulky. Next, the threshold memristor emulator developed in [43] is specifically for the digital application. However, the utilization of large number of components makes the structure as complex.

The majority of the existing emulators contains non-linear elements such as Diodes [33,17,18], and analog multiplier [19–24,26–28,40,41,44]. The non-linear circuitry further increases the complexity as well as power consumption. However, very few multiplier-less emulators have existed but they have some other disadvantages such as low operating frequency, use of floating passive elements, and complex structures. The realization of multiplier-less memristor emulator using CBTA and two capacitors in [45]; Voltage Differencing Current Conveyor (VDCC), one grounded capacitor and a voltage-controlled resistor using two PMOS transistors in [46]; VDTA (Voltage Differencing Transconductance Amplifier) and a MOSFET based grounded capacitor in [47]. However, excess passive components unnecessarily increase the chip area and power consumption.

This paper presents a novel FQAM circuit and its applications using a single active element CDTA and two NMOS. Unlike other existing work in the literature, this circuit provides both voltage and trans-conductance mode outputs simultaneously. It has additional features such as a fully active, cascadable, and configurable structure. Further, the FQAM circuit is configured to develop a memristor emulator based on the proposed mathematical analogy (as shall be discussed later). The proposed memristor circuit contains active elements (one CDTA, two NMOS, and one Inverting Voltage buffer) and only one grounded capacitor. However, the grounded capacitor can be easily implemented by MOS-cap which makes the circuit suitable for monolithic integration [47]. It offers tunability using trans-conductance gain of the CDTA block. Also, the proposed memristor emulator circuit doesn't contain any additional multiplier block. In last, the capacitor-less version of the memristor emulator has been presented.

2. Circuit description

2.1. CDTA

The CDTA is a five-terminal active device and can be considered as the combination of a current differencing unit (CDU) and a dual-output operational transconductance amplifier (DO-OTA). The CMOS implementation of CDTA is shown in Fig. 1 whose symbolic representation is given in Fig. 2. The P and N are the low-impedence input terminals, $X+$ and $X-$ are the high-impedence output terminals while Z is an auxiliary terminal which is used to establish the relationship between the input and output currents. The port relationship of CDTA can be characterized in matrix form as

$$\begin{bmatrix} V_P \\ V_N \\ I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & -1 & 0 \\ 0 & 0 & g_m \\ 0 & 0 & -g_m \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_Z \end{bmatrix} \tag{1}$$

By simplifying the matrix, subsequent relations are obtained. These can be refereed to as the defining equations of CDTA.

$$\begin{aligned} V_P, \quad V_N &= 0, \quad I_Z \\ &= I_P - I_N, \quad I_{X+} \\ &= g_m V_Z, \quad I_{X-} \\ &= -g_m V_Z \end{aligned} \tag{2}$$

where g_m denotes the transconductance gain whose mathematical expression can be described as follows:

$$g_m = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_{9,10} I_b} \tag{3}$$

where μ_n denotes the channel mobility; C_{ox} is the gate oxide capacitance per unit area; W/L is the aspect ratio of the MOS transistor M_9 or M_{10} and I_b is the bias current used for controlling the trans-conductance gain.

2.2. Proposed FQAM

The proposed FQAM employing single CDTA and two NMOS transistors is shown in Fig. 3. Under operating condition, the two external NMOS M_P & M_N are assumed to be operated in linear region. The generalized expression of drain current for the NMOS in the linear (triode) region is stated as below

$$I_D = K_N \frac{W}{L} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{4}$$

where, $V_{DS} < V_{GS} - V_{tn}; V_{GS} > V_{tn}$, parameter K_N, W and L denotes the transconductance, width and length of the channel for the NMOS, respectively; V_{tn} is the threshold voltage while V_{GS}, V_{DS} are the terminal voltages. Since, the source terminals of both the externally connected NMOS are virtually grounded due to intrinsic property of CDTA ($V_P = V_N = 0$), so using Eq. (4), the currents I_P & I_N can be expressed as

$$I_P = K_N \frac{W}{L} \left[(V_2 + V_G - V_{tn}) V_1 - \frac{V_1^2}{2} \right] \tag{5}$$

$$I_N = K_N \frac{W}{L} \left[(V_G - V_{tn}) V_1 - \frac{V_1^2}{2} \right] \tag{6}$$

Now, using port relationship of CDTA ($I_Z = I_P - I_N$), the output voltage and current V_0 & I_0 respectively can be obtained as

$$V_0 = \frac{1}{g_m} \cdot I_Z = \frac{1}{g_m} \cdot K_N \frac{W}{L} V_1 V_2 \tag{7}$$

$$I_0 (= I_{X+}) = g_m V_0 = K_N \frac{W}{L} V_1 V_2 \tag{8}$$

From Eqs. (7) and (8), it can be observed that the circuit produces multiplier output in voltage and current form with multiplication constant $1/g_m K_N \frac{W}{L}$ and $K_N \frac{W}{L}$ respectively. It can be seen that this circuit produces trans-conductance as well as voltage mode output simultaneously without the need of an extra resistor. Further, to test the functionality of the proposed FQAM circuit, the two input signals are assumed as, $V_1 = V_m Sin 2\pi f_1 t$ and $V_2 = V_m Sin 2\pi f_2 t$. So, using Eq. (7), the mathematical expression can be obtained as

$$V_0 = \left(\frac{1}{g_m} \cdot K_N \frac{W}{L} \right) \cdot \frac{{V_m}^2}{2} \left[Cos 2\pi (f_1 - f_2) t - Cos 2\pi (f_1 + f_2) t \right] \tag{9}$$

From Eq. (9), it is noted that the output contains only two frequency components namely, $(f_2 \pm f_1)$. But, the practical circuit also contains undesired inter-modulation products at frequencies given by

$$\sum_{p=1}^{p=\infty} \sum_{q=1}^{q=\infty} (pf_2 \pm qf_1) - (f_2 \pm f_1) \tag{10}$$

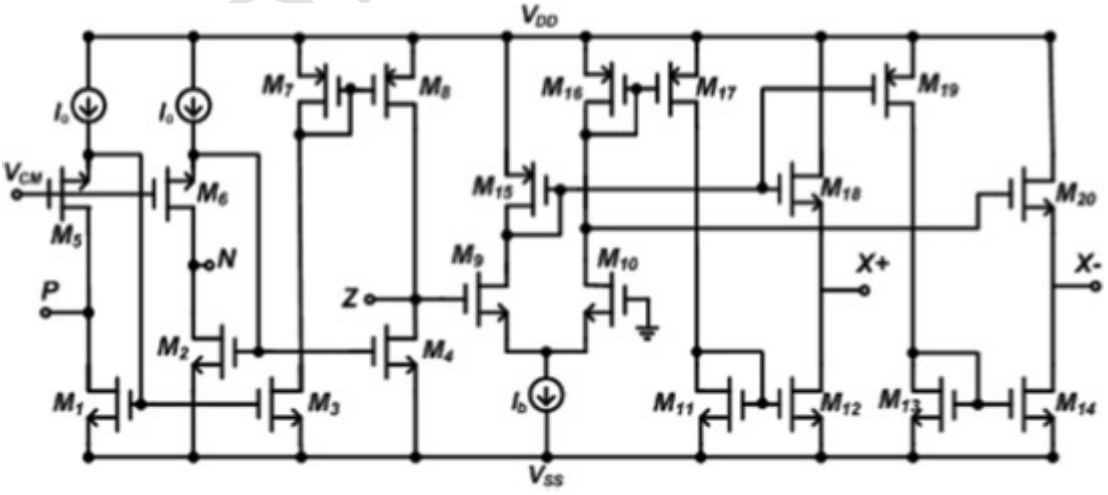


Fig. 1. CMOS implementation of CDTA [48].

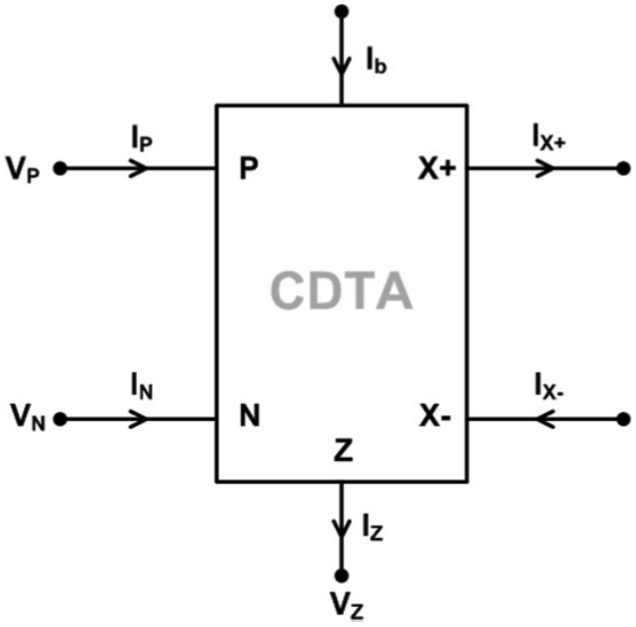


Fig. 2. Symbolic representation of CDTA.

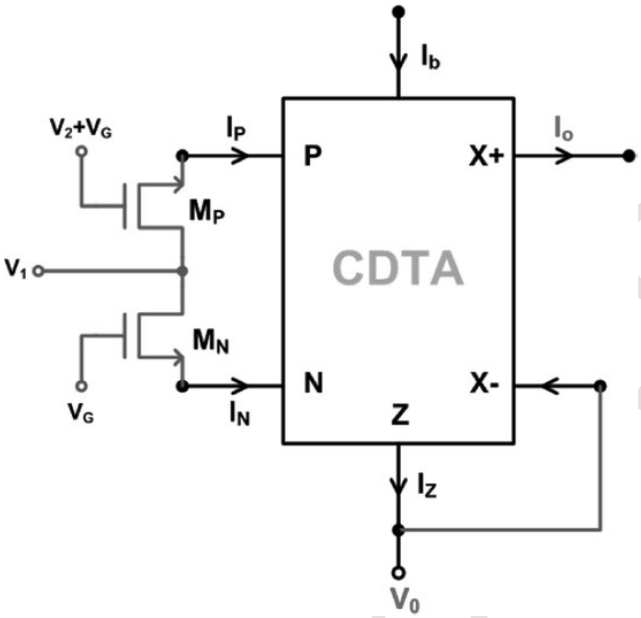


Fig. 3. Proposed FQAM Circuit.

In Eq. (10), the undesired frequency terms up to $p,q = 3$ are considered because they mainly contribute to the inter-modulation distortion (IMD). Hence, it is necessary to estimate the adjacent undesired inter-modulation products.

2.3. Proposed memristor emulator

2.3.1. Background theory

The proposed memristor emulator circuit shown in Fig. 4 is based on multiplier topology presented in previous section. The realization of the memristor emulator utilized a proposed FQAM, inverting voltage buffer which is shown in Fig. 5 [49] and a grounded capacitor. The background theory for the development of the memristor emulator circuit is based on mathematical analogy between FQAM and memristor. The general expression for the flux-controlled memristor is stated as

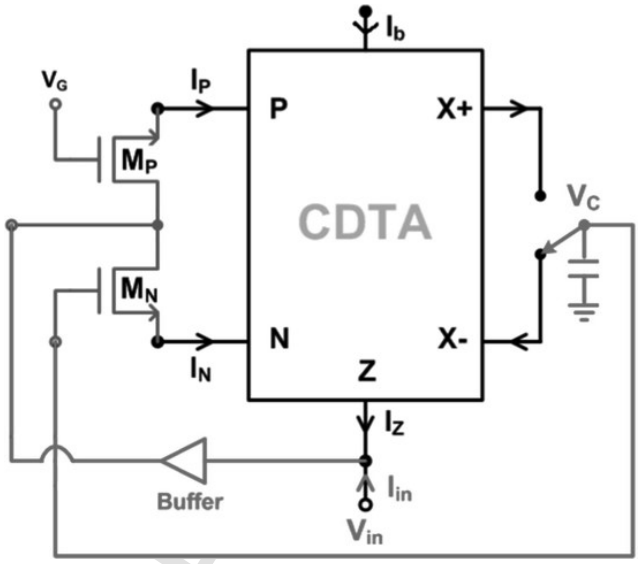


Fig. 4. Proposed Memristor Emulator Circuit.

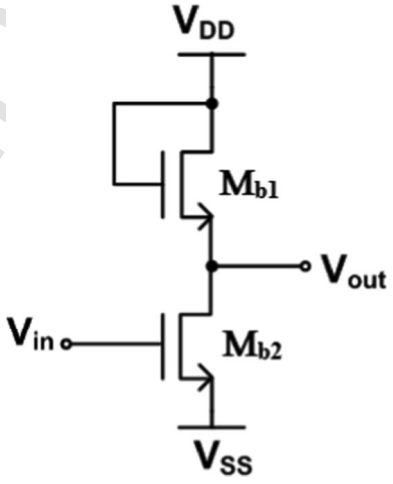


Fig. 5. Inverting voltage buffer using two NMOS Transistors [49].

$$I_{in} = \left(K_1 + K_2 \int V_{in}\right) V_{in} \tag{11}$$

Now, in order to understand the analogy, let us compare the generalized expression of memristor in Eq. (11) with the output of the FQAM circuit in Eq. (8). It is observed that the basic difference between the two expressions is the memristor emulator circuit contains an offset. Now, it can be achieved simply by removing the dc voltage V_G which was actually added with the V_2 in FQAM circuit for the removal of dc offset. So, the multiplier output in Eq. (8) is modified accordingly as:

$$I_0 = (K_1 + K_2 \cdot V_2) V_1 \tag{12}$$

Where, $K_1 = K_N \frac{W}{L} V_G$ and $K_2 = K_N \frac{W}{L}$ are constants. Now, for the case where, $V_1 = V_{in}$ and $V_2 = \int V_{in}$, the Eq. (11) and (12) shows the analogy between FQAM and memristor circuits.

2.3.2. Mathematical expression

The current entering into the P and N-terminals are expressed as

$$I_P = K_N \frac{W}{L} \left[-(V_G - V_{tn}) V_{in} - \frac{V_{in}^2}{2} \right] \tag{13}$$

$$I_N = K_N \frac{W}{L}\left[-(V_C - V_{tn})V_{in} - \frac{V_{in}^2}{2}\right] \tag{14}$$

The voltage across capacitor, V_C is written as

$$V_C = \pm\frac{g_m}{C}\int V_{in}dt = \pm\frac{g_m}{C}\cdot\phi \tag{15}$$

where, (+) and (−) signs represent the polarity of voltage across capacitor when it is connected to X+ and X− terminals, respectively. The ϕ denotes the time integral of input voltage or accumulated flux.

As according to the port relationship of CDTA,

$$I_Z = I_P - I_N \tag{16}$$

Now, the voltage buffer is also used to block the current division at port-Z in Fig. 4. The aspect ratio of mosfet's in voltage buffer are assumed so as it offers infinitely large resistance and hence holds the current relation below

$$I_{in} = -I_Z \tag{17}$$

Now using above equations, the current-voltage relationship and the expression for the memductance (reciprocal of memristance) can be deduced as

$$I_{in} = \left(K_N \frac{W}{L}V_G \pm K_N \frac{W}{L}\frac{g_m}{C}\phi\right)V_{in} \tag{18}$$

$$W(\phi) = \left(K_N \frac{W}{L}V_G \pm K_N \frac{W}{L}\frac{g_m}{C}\phi\right) \tag{19}$$

The Eqs. (18) and (19) represents the I-V relationship and expression of memductance for the proposed flux controlled memristor emulator circuit. Here, + (switch connected to $X+$) and − (switch connected to X−) sign represents the incremental and decremental configuration, respectively. These expression can be compared with the equations of generalized linear ion drift model of memristor. Further, in order to understand the frequency dependent behavior of the memristor, a sinusoidal excitation as $V_{in}(t) = VmSin\omega t$ where, ω is the frequency in rad/s and then the Eqs. (18) and (19) is modified accordingly as

$$I_{in} = \left(K_N \frac{W}{L}V_G \pm K_N \frac{W}{L}g_m V_m \frac{Cos(\omega t - \pi)}{\omega C}\right)V_{in} \tag{20}$$

$$W(\phi) = \left(K_N \frac{W}{L}V_G \pm K_N \frac{W}{L}g_m V_m \frac{Cos(\omega t - \pi)}{\omega C}\right) \tag{21}$$

The above Eqs. (20) and (21) shows the behavior of the proposed memristor emulator circuit in frequency domain. It is observed that these equations consist of two parts namely linear time-invariant and time-variant which decides the slope and area of the current-voltage hysteresis plot respectively. So, increase in the operating frequency decreases the time-variant part, hence reduces the loop area. Finally, hysteresis loop converges to linear shape for higher values. Now, the correlation factor (γ) can be defined as the ratio of the amplitudes of linear time-variant and invariant part of memductance in Eq. (21) is expressed as:

$$\gamma = \frac{g_m V_m}{wCV_G} = \frac{1}{\tau f} = \frac{T}{\tau} \tag{22}$$

where, τ represents the time constant and f is the frequency of excitation of the emulator circuit. Then, using Eq. (22), the time constant (τ) of the emulator circuit is expressed as

$$\tau = \frac{2\pi CV_G}{g_m V_m} \tag{23}$$

From Eq. (22), the Time period can be obtained as,

$$T = \frac{1}{f} = \frac{2\pi\gamma CV_G}{g_m V_m} \tag{24}$$

From, Eq. (22), (23), it can be concluded that the memristor behavior in frequency domain is governed by the frequency-to-amplitude ratio of the excitation as well as the time constant of the proposed emulator circuit. Further, the range of γ is generalized to predict the behavior of the memductance for the change in frequency and the amplitude of the excitation is listed below:

Case-1: When frequency is variable, V_m fixed

- $\gamma \to 0$, when $f \to \infty$, the linear time-variant terms governs the behavior of the memductance. In other words, hysteresis loop achieves the linear shape.
- $\gamma \to 1$, when $f \to 1/\tau$, it maximizes the pinched hysteresis loop.
- $\gamma \geqslant 1$, when $f \leqslant 1/\tau$, it concludes that the time period (T) is greater than $1/\tau$ and hence the circuit will lost the pinched hysteresis behavior.

Case-2: Frequency is fixed with V_m variable

- $\gamma \to 0$, when V_m decreases, the linear time-variant terms govern the behavior of the memductance. In other words, the hysteresis loop achieves the linear shape.
- $\gamma \to 1$, when V_m is monotonically increased, so for this condition, the pinched hysteresis loop will be maximized.
- $\gamma \geqslant 1$ for large values of V_m, the circuit will lose the pinched hysteresis behavior. It means that time constant τ is modified while the time period (T) is constant.

So, to ensure the behavior of the pinched hysteresis characteristics for the situations mentioned above, it is necessary to update the time constant accordingly. At the same time, the value of γ should be kept between 0 and 1 i.e. $0 \leqslant \gamma \leqslant 1$. Further, it can be noted that the time constant depends on the trans-conductance (g_m), hence its value can be varied by the controlled current thus, enables the circuit with the electronically controllable feature.

So, based on this explanation, the minimum frequency to avoid the negative memductance value is obtained according to the condition, $\gamma \leqslant 1$.

$$w \geqslant \frac{g_m V_m}{CV_G} \tag{25}$$

Hence, it is justified that the proposed memristor emulator circuit obeys the critical fingerprints of memristor for the condition $0 \leqslant \gamma \leqslant 1$.

2.4. Mismatch analysis

2.4.1. Effect of threshold voltage difference

In the previous analysis given for the proposed FQAM in Fig. 3 and Memristor Emulator in Fig. 4, the threshold voltage (V_m) of the NMOS transistors M_P and M_N are assumed matched. But, practically it is difficult to fabricate the matched transistors. So, for the case where mismatch in threshold voltages of two NMOS (M_P and M_N) exists, the mathematical expression of FQAM is modified accordingly as

$$V_0 = \frac{1}{g_m}\cdot K_N \frac{W}{L}V_1 V_2 - \frac{1}{g_m}\cdot K_N \frac{W}{L}(V_{tnP} - V_{tnN})V_1 \tag{26}$$

$$I_0 = K_N \frac{W}{L}V_1 V_2 - K_N \frac{W}{L}(V_{tnP} - V_{tnN})V_1 \tag{27}$$

where V_{tnP} & V_{tnN} are the threshold voltages of transistors M_P and M_N respectively. Now, from Eq. (26) and (27), it can be seen that outputs are affected due to mismatch in threshold voltages. Also, it is to be

noted that for lesser difference in threshold voltages, the output expressions approaches towards ideal form as in Eqs. (7) and (8). Subsequently, care must be taken while selecting transistors i.e. should have close values of threshold.

Further, the effect of mismatch analysis on the Memristor Emulator circuit can be observed as

$$I_{in} = \left(K_N \frac{W}{L}(V_G + V_{tnP} - V_{tnN}) \pm K_N \frac{W}{L}\frac{g_m}{C}\phi\right) V_{in} \tag{28}$$

$$W(\phi) = K_N \frac{W}{L}(V_G + V_{tnP} - V_{tnN}) \pm K_N \frac{W}{L}\frac{g_m}{C}\phi \tag{29}$$

Eq. (28) shows the current–voltage relationship for the memristor emulator in case of threshold mismatching. Now, it can be observed that difference in threshold voltage gets added/subtracted to the time-invariant term, so it affects the slope of hysteresis loop without affecting the basic fingerprints of the memristor.

2.4.2. Effect of W/L difference

For the ideal case in previous section, it is considered that the aspect ratios of the external MOSFETs M_P and M_N should be same but practically some mismatch exists, can be evaluated in this section.

The multiplier output voltage and current can be written respectively as

$$V_0 = \frac{K_N}{g_m}\left[\left(\frac{W}{L}\right)_1 \cdot V_2 V_1 + \left\{\left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2\right\}(V_G - V_{tn})V_1\right] \tag{30}$$

$$I_0 = K_N\left[\left(\frac{W}{L}\right)_1 \cdot V_2 V_1 + \left\{\left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2\right\}(V_G - V_{tn})V_1\right] \tag{31}$$

From Eq. (30) and (31), it can be noted that output expression contains an additional offset which is added to the multiplication output. But, analyzing the expression, it is understood that the offset is actually of low value, hence doesn't affect the multiplier performance.

Next, the effect of aspect ratio mismatch on the proposed memristor emulator circuit can be obtained as

$$I_{in} = K_N\left[\left(\frac{W}{L}\right)_2 V_G + \left\{\left(\frac{W}{L}\right)_2 - \left(\frac{W}{L}\right)_1\right\} V_{tn} \pm \left(\frac{W}{L}\right)_1 \cdot \frac{g_m}{C}\phi\right] V_{in} \tag{32}$$

$$W(\phi) = K_N\left[\left(\frac{W}{L}\right)_2 V_G + \left\{\left(\frac{W}{L}\right)_2 - \left(\frac{W}{L}\right)_1\right\} V_{tn} \pm \left(\frac{W}{L}\right)_1 \cdot \frac{g_m}{C}\phi\right] \tag{33}$$

The simplified equations obtained above represents the current-voltage relationship and the memductance for the case when aspect ratios of two external MOSFETs M_P and M_N are not matched. It can be noted from the equation that the constant value is added to the linear time-invariant term which slightly affects the slope of the characteristics without altering the signature characteristics.

2.5. Non-ideal and parasitic analysis

The effects of the non-ideal transfer gains on the proposed circuits shown in (Fig. 3 and 4) are analyzed. The non-idealities in CDTA is characterized by the following port relationships.

$$\begin{aligned} I_Z &= \alpha_P I_p - \alpha_N I_n; \quad I_{X+} \\ &= \beta_1 g_m V_Z; \quad I_{X-} \\ &= -\beta_2 g_m V_Z, \quad V_P, V_N \\ &= 0 \end{aligned} \tag{34}$$

where α_P, α_N denotes the current transfer gain from terminals P,N to terminal-Z respectively while β_j (j = 1,2) represents the transconductance inaccuracy factor from Z to $X+$, $X-$ terminal. More specifically, $\alpha_P = (1 - \epsilon_P), \alpha_N = (1 - \epsilon_N)$ where $\epsilon_P(|\epsilon_P| \ll 1), \epsilon_N(|\epsilon_N| \ll 1)$ is the current tracking error and $\beta_j = (1 - \delta_j)$ where $\delta_j(|\delta_j| \ll 1)$ is the tracking error in transconductance of the CDTA.

The non-ideal analysis for the multiplier circuit yields the voltage and current output as

$$V_0 = \frac{1}{\beta_2 g_m} \cdot K_N \frac{W}{L}\left[\alpha_P V_1 V_2 + (\alpha_P - \alpha_N)(V_G - V_{tn})V_1 - (\alpha_P - \alpha_N)\frac{V_1^2}{2}\right] \tag{35}$$

$$I_0 = \frac{\beta_1}{\beta_2} \cdot K_N \frac{W}{L}\left[\alpha_P V_1 V_2 + (\alpha_P - \alpha_N)(V_G - V_{tn})V_1 - (\alpha_P - \alpha_N)\frac{V_1^2}{2}\right] \tag{36}$$

The above Eq. (35), (36) shows the exact expression in case of non-unity transfer gains. But, it can be approximated after neglecting the terms containing $(\alpha_P - \alpha_N)$ because α_P, α_N are nearly equal to one (ideally 1).

$$V_0 = \left(\frac{\alpha_P}{\beta_2 g_m} \cdot K_N \frac{W}{L}\right) V_1 V_2 \tag{37}$$

$$I_0 = \left(\frac{\alpha_P \beta_1}{\beta_2} \cdot K_N \frac{W}{L}\right) V_1 V_2 \tag{38}$$

Now, it is observed from the Eqs. (37) and (38), the multiplier outputs are slightly affected by the non-idealities. Similarly, the effect of non-idealities on the memristor emulator circuit can be summarized as

$$I_{in} = K_N \frac{W}{L}\left(\alpha_N V_G + (\alpha_P - \alpha_N)V_{tn} \pm \beta_1 \alpha_P \cdot \frac{g_m}{C}\phi\right) V_{in} - K_N \frac{W}{L}(\alpha_P - \alpha_N)\frac{V_{in}^2}{2} \tag{39}$$

The above equation can be simplified by neglecting the terms containing $(\alpha_P - \alpha_N)$, then current-voltage relationship and its corresponding memductance can be obtained as

$$I_{in} = \left(\alpha_N K_N \frac{W}{L} V_G \pm \beta_1 \alpha_P \cdot K_N \frac{W}{L}\frac{g_m}{C}\phi\right) V_{in} \tag{40}$$

$$W(\phi) = \left(\alpha_N K_N \frac{W}{L} V_G \pm \beta_1 \alpha_P \cdot K_N \frac{W}{L}\frac{g_m}{C}\phi\right) \tag{41}$$

From Eqs. (40) and (41), it can be seen that the magnitude of linear time-invariant and time-variant terms gets slightly decreased due to non-unity transfer gains. So, the slope and area of the hysteresis loop may reduce slightly without affecting signature characteristics.

$$\gamma = \frac{\beta_1 \alpha_P g_m V_m}{\alpha_N \omega C V_G} \tag{42}$$

$$\tau = \frac{2\pi \alpha_N C V_G}{\beta_1 \alpha_P g_m V_m} \tag{43}$$

Next, in order to observe the high frequency limitation of the proposed circuits, the parasitics of CDTA with its effects have been studied (shown in Fig. 6).

- R_P , R_N are parasitic resistance (typically few ohms) value appeared at high frequency at the port P, N respectively.

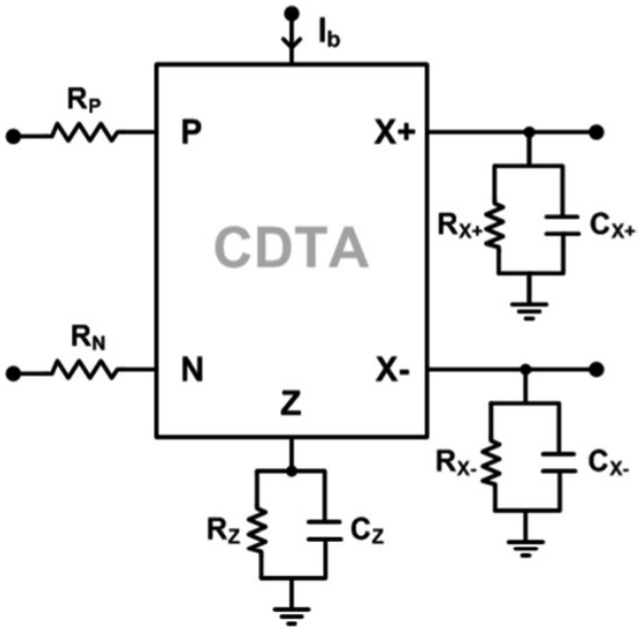


Fig. 6. Representation of CDTA block with parasitic components.

- $R_Z//(1/sC_Z)$ is the parasitic impedence (typically of the order of mega-ohms) appeared at port-Z on high frequencies.
- $R_{X+}//(1/sC_{X+})$ is the parasitic impedence (typically of the order of mega-ohms) appeared at port X+ on higher frequencies.
- $R_{X-}//(1/sC_{X-})$ is the parasitic impedence (typically of the order of mega-ohms) appeared at port X- on higher frequencies.

Considering the parasitic effects characterized above, the mathematical expression for the proposed FQAM circuit shown in Fig. 3 can be reanalyzed as below.

$$V_0 = K_N \frac{W}{L}\left[\frac{(1+sR'C')}{R'+g_m(1+sR'C')}\right]\left[V_2(V_1 - I_P R_P) - (V_G - V_t)(I_P R_P - I_N R_N)\right] \tag{44}$$

$$I_0 = K_N \frac{W}{L}\left[\frac{g_m(1+sR'C')}{R'+g_m(1+sR'C')}\right]\left[V_2(V_1 - I_P R_P) - (V_G - V_t)(I_P R_P - I_N R_N)\right] \tag{45}$$

where, $R' = R_Z//R_{X-}$ and $C' = C_Z + C_{X-}$. The Eqs. (44) and (45) shows the parasitic effects on multiplier outputs which appears on higher frequencies. Also, for the simplification of the expressions, the terms containing factor $(I_P R_P - I_N R_N)$ can be neglected because the magnitude of $I_P R_P$ and $I_N R_N$ are nearly equal and small (ideally 0).

$$V_0 = K_N \frac{W}{L}\left[\frac{(1+sR'C')}{R'+g_m(1+sR'C')}\right]\left[V_2(V_1 - I_P R_P)\right] \tag{46}$$

$$I_0 = K_N \frac{W}{L}\left[\frac{g_m(1+sR'C')}{R'+g_m(1+sR'C')}\right]\left[V_2(V_1 - I_P R_P)\right] \tag{47}$$

where, $\left[\frac{(1+sR'C')}{R'+g_m(1+sR'C')}\right] \Rightarrow (1/g_m)//R_Z//R_{X-}//(1/s(C_Z + C_{X-}))$ (order of few K $\longrightarrow 1/g_m$ ω). Hence, Eqs. (46) and (47) reduces to ideal form in Eqs. (7) and (8), respectively. Also, it can be noted from the Eqs. (46) and (47), the multiplier outputs contains a very low offset which can be considered negligible, so the presence of parasitics at higher frequencies doesn't affect the performance of the proposed FQAM circuit.

Similarly, on considering the effect of parasitics at high frequencies, the memristor emulator circuit shown in Fig. 4 is reanalyzed. For obtaining the mathematical expressions in simplified form, the assumptions $V_{in} \gg |I_P R_P|, |I_N R_N|$ and $(I_P R_P - I_N R_N) \approx 0$ have been considered.

$$I_{in} = \left[\left(K_N \frac{W}{L} V_G + \frac{1+sR_Z C_Z}{R_Z}\right) - K_N \frac{W}{L} \cdot \frac{g_m R_{X-}}{(1+sR_{X-}C'')} V_{in}\right] V_{in} \tag{48}$$

$$W(\phi) = \left(K_N \frac{W}{L} V_G + \frac{1+sR_Z C_Z}{R_Z}\right) - K_N \frac{W}{L} \cdot \frac{g_m R_{X-}}{(1+sR_{X-}C'')} V_{in} \tag{49}$$

where, $C'' = C + C_{X-}$; the Eqs. (48) and (49) shows the current-voltage relationship and the expression for memductance due to the effect of parasitics at high frequencies. Here, the equivalent admittance at port-Z i.e. $(1+sR_Z C_Z)/R_Z \Rightarrow sC_Z + \frac{1}{R_Z} \approx 0$; the equivalent impedance at port-(X−) i.e. $\frac{R_{X-}}{(1+sR_{X-}C'')} \Rightarrow R_{X-}//\frac{1}{sC_{X-}}//\frac{1}{sC} \approx \frac{1}{sC}$. So, for these approximations, Eqs. (48) and (49) has the similar form to ideal case in Eq. (18). Hence, it can be concluded that due to the slight change in the linear time-invariant and time-variant terms, the slope and the loop area may affected but there is no deviation in the signature characteristics.

3. Simulation results

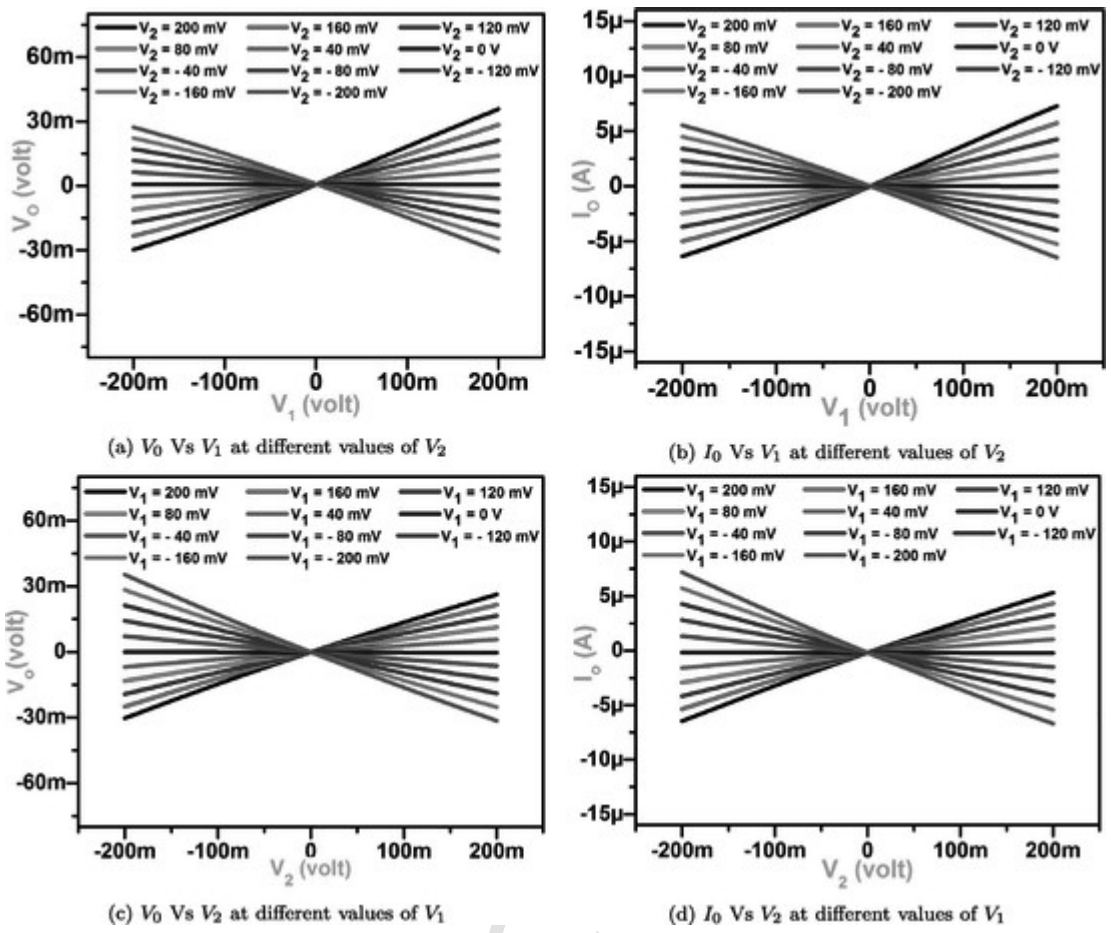
The simulation verification of the proposed FQAM and memristor emulator circuits have been demonstrated using HSPICE program. The realization of the proposed circuits have been done using active block CDTA whose CMOS implementation and symbolic representation is shown in Figs. 1 and 2, respectively. The internal structure of CDTA uses TSMC 0.25 μm CMOS technology with the aspect ratio as according to the Table 1 [48]. For the better performance of the CDTA block, the supply voltage of ±1.2 V is selected and the other constant sources used are $V_{CM} = 0.2$ V; $I_o = 100$ μA. The performance parameters obtained are $\alpha_P = \alpha_N = 1.0055$, $g_m = 208.8$ μA/V for the bias current of 50 μA.

3.1. FQAM circuit

The Fig. 3 shows the FQAM circuit, contains an external MOSFET's whose aspect ratios are: $(W/L)_{M_P} = (W/L)_{M_N} = (1\ \mu m/1\ \mu m)$. The dc voltage $V_G = 0.85$ V is used for the multiplier operation. To examine the linearity range of the proposed FQAM, dc characteristics are shown in Fig. 7. The Fig. 7(a-b) show the outputs (V_o&I_o) versus dc input V_1 in its linear range of −200 mV to +200 mV, while the other input V_2 is stepped between −200 mV to +200 mV with 40 mV step size. Fig. 7(c-d) show the different outputs obtained by interchanging the two inputs V_1 and V_2. The results show excellent linearity and hence confirm the functionality of the proposed FQAM circuit. Fig. 8 shows the frequency response of the proposed FQAM circuit. The result of ac analyses is obtained for voltage V_1 equal to 200 mV dc while V_2 is taken as AC source having amplitude 200 mV. The result shows −3 dB band-

Table 1
Aspect ratio of 0.25 μm CMOS transistors in CDTA implementation [48].

Transistors	W (μm)	L (μm)
$M_1 - M_8$	20	1
$M_9 - M_{10}$	5	1
$M_{11} - M_{14}$	3	1
$M_{15} - M_{20}$	5	1



(a) V_0 Vs V_1 at different values of V_2

(b) I_0 Vs V_1 at different values of V_2

(c) V_0 Vs V_2 at different values of V_1

(d) I_0 Vs V_2 at different values of V_1

Fig. 7. DC characteristics for the proposed Four Quadrant Analog multiplier.

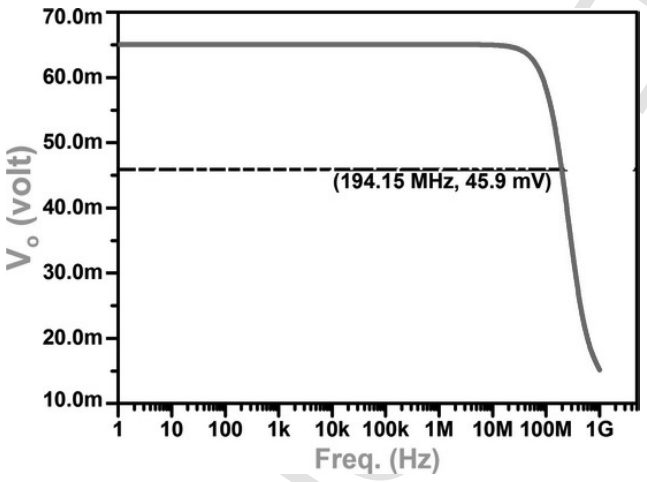


Fig. 8. Frequency response for the proposed multiplier.

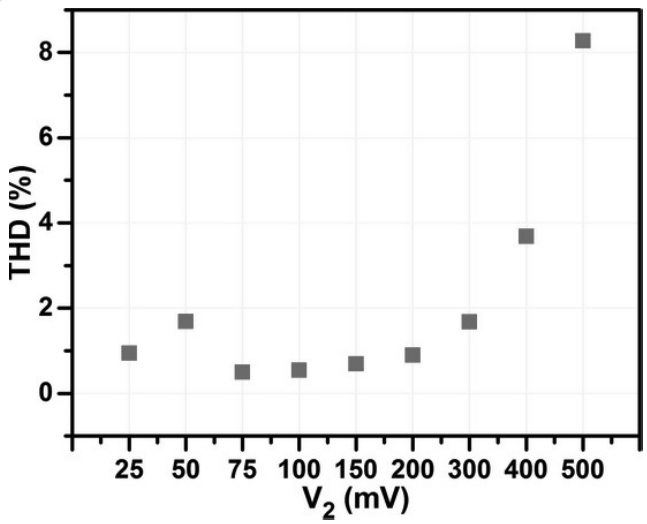


Fig. 9. Variation in THD (%) with the amplitude of the input signal V_2.

width of 197.16 MHz, which can be considered as adequately high. Next, to observe the non-linearity in terms of Total Harmonic Distortion (THD), V_2 is taken as a 10 MHz signal of variable amplitude while V_1 is a fixed dc signal of 200 mV. Fig. 9 shows the THD (%) variation for the different amplitudes of V_2. It can be seen from this graph that in the linear range of V_2, the THD values are less than 1.68 %, which validates its excellent performance. Next, due to the presence of non-linearities in the circuit, the Inter-modulation Distortion (IMD) may occurs. So, to observe its effects, two input signals having equal amplitude of 100 mV but different frequencies of 1 kHz and 30 kHz are used.

Table 2 shows the amplitude of each frequency component expressed as inter-modulation products. Ideally, the spectrum should contain the components only at frequencies, $f_1 - f_2 = 29$ KHz, $f_1 + f_2 = 31$ KHz. But, practically it also contains unwanted components which contributes to the Inter-modulation Distortion (IMD). The lower decibel values of undesired inter-modulation products signify lesser IMD.

Table 2
Inter-modulation products for the proposed amplitude modulator.

Freq. (kHz)	1	2	28	**29**	30	**31**	32	58	59	60	61	62	88	89	90	91	92
Mag. (dB)	−24.2	−66.4	−35.4	**0**	−29.1	**0**	−35.4	−78.5	−33.6	−54.9	−33.6	−74.5	−71.1	−44.2	−63.6	−44.3	−73.4

3.2. Memristor emulator

In this section, the memristor emulator circuit using the FQAM topology has been developed, as shown in Fig. 4. It also employs an inverting voltage buffer [49], as shown in Fig. 5, consists of two NMOS transistors whose aspect ratios are $(W/L)_{M_{b1}} = (W/L)_{M_{b2}} = (10\ \mu m/1\ \mu m)$. Now, for the emulator circuit to behave like a memristor, its i-v curve should follow the three basic fingerprints of the generalized memristor [50]. So, the behavior of the proposed emulator circuit has been investigated for the sinusoidal excitation of the wider frequency range. Fig. 10 shows the simulation result in the form of a pinched hysteresis loop for an input signal of 50 mV amplitude and variable frequency from 1 Hz to 10 MHz. From Eq. (20), it is noted that the linear time-varying term follows an inverse relationship with the frequency.Hence, with the increase in frequency, the area of the loop should be decreased. It has been observed in Fig. 10(a-d) that on increasing the operating frequency, the loop area decreases and finally attains a linear current-voltage relationship. Also, all the sub-figures have fixed value of the frequency-capacitance product, which results in similar hysteresis characteristics as suggested by theoretical analysis in Eq. (20). But, this frequency-capacitance relationship is not effective for further increment in frequencies (above 1 MHz) because the parasitic capacitances have appeared on higher frequencies, as explained by Eq. (49). Fig. 11 shows the hysteresis characteristics at higher frequencies (10, 20, 100, 200 MHz), all the curves have different capacitance values which are not selected according to the constant frequency-capacitance product. Also, it can be noted from Fig. 11(c,d), the hysteresis characteristics were not pinched at the origin, which is due to the presence of the parasitic resistance R_P, R_N at higher frequencies. So, some offset voltages have been developed across terminals P,N, which creates a non-zero voltage at source terminals of external MOSFETs (M_P, M_N). However, this deviation can be compensated using dc sources between the external MOSFETs and the CDTA block. Also, the linear time-varying term in Eq. (20) contains capacitance in the denominator; hence for higher values of capacitance keeping the frequency constant, the loop area should decrease, which is shown in Fig. 12. So, it can be concluded that the capacitance value should be adjusted according to the range of operating frequency. Now, it is examined that the obtained curves follow the signature characteristics and hence validates the proposed design as a memristor emulator circuit.

Further, the electronically controllable feature of the proposed emulator circuit has been demonstrated in Fig. 13. According to Eq. (3), the increase in bias current increases the transconductance gain (g_m) of CDTA, which augments the time-variant term of Eq. (20). So, the area of the hysteresis loop and hence the average memristance value is more

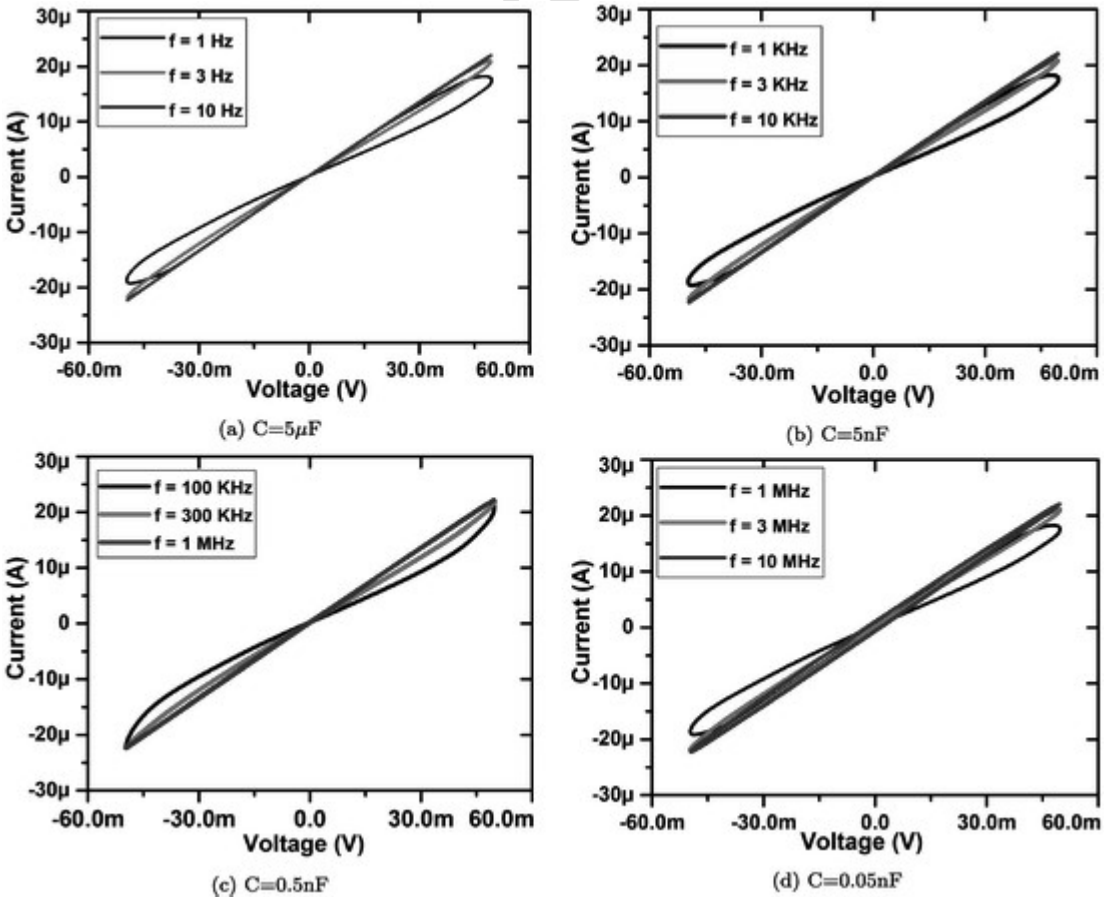


Fig. 10. Hysteresis characteristics for the proposed Memristor Emulator.

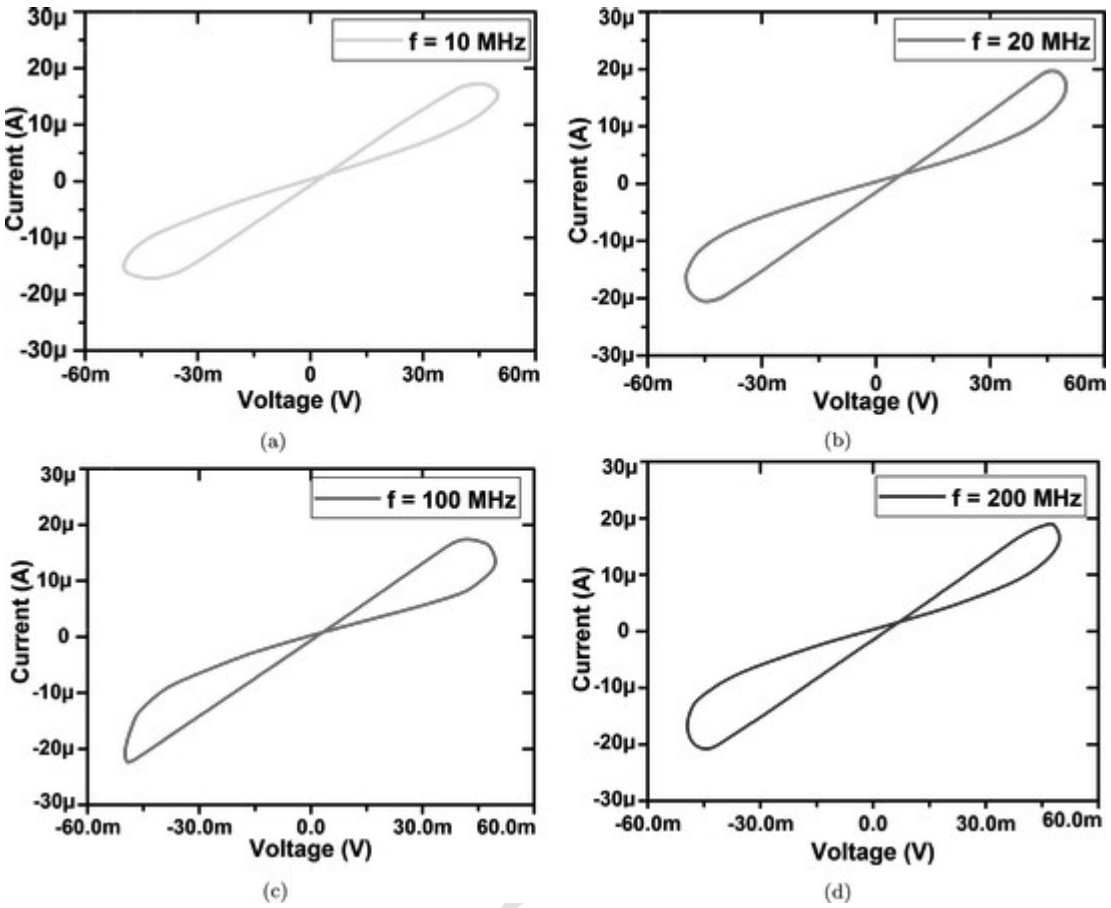


Fig. 11. Hysteresis characteristics at higher frequencies.

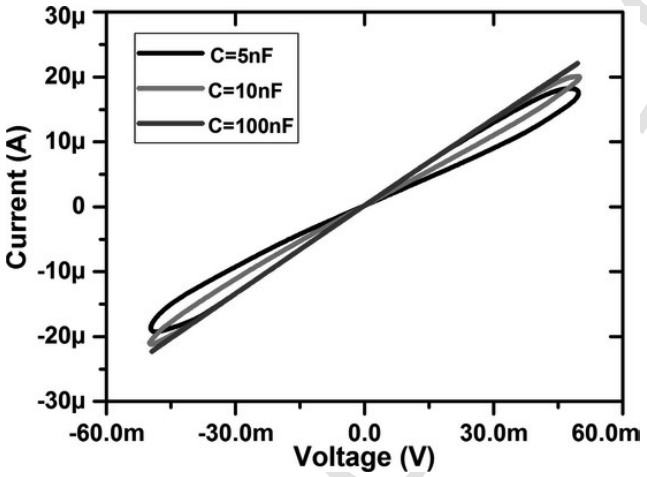


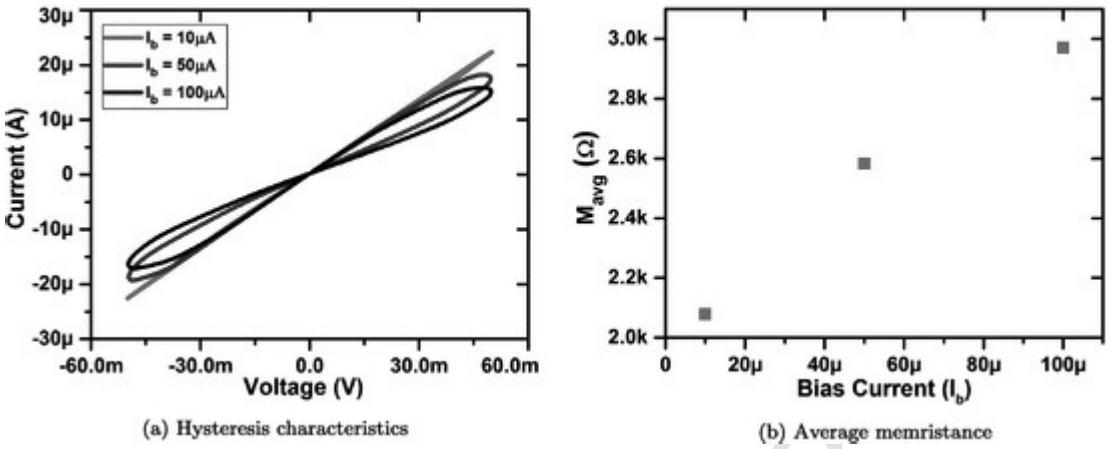
Fig. 12. Hysteresis characteristics for variable capacitance at 1 kHz.

for the higher values of I_b, as depicted in Figs. 13a and b, respectively. Hence, the g_m versus I_b relationship inherited tunability to the proposed circuit, so it is fancied to use it as a controlled weight in neuromorphic circuits.

Next, the effect of the variation in maximum amplitude (V_m) of sinusoidal excitation on the proposed circuit behavior has been demonstrated in Fig. 14. It is evident from Eq. (20) that the variable term varies linearly with the maximum amplitude, so any change in V_m affects the area of the loop. Hence, for a linear increase in V_m from 50 mV to 150 mV, the area of the hysteresis loop and average memristance value increases, as shown in Fig. 14(a) & (b), respectively.

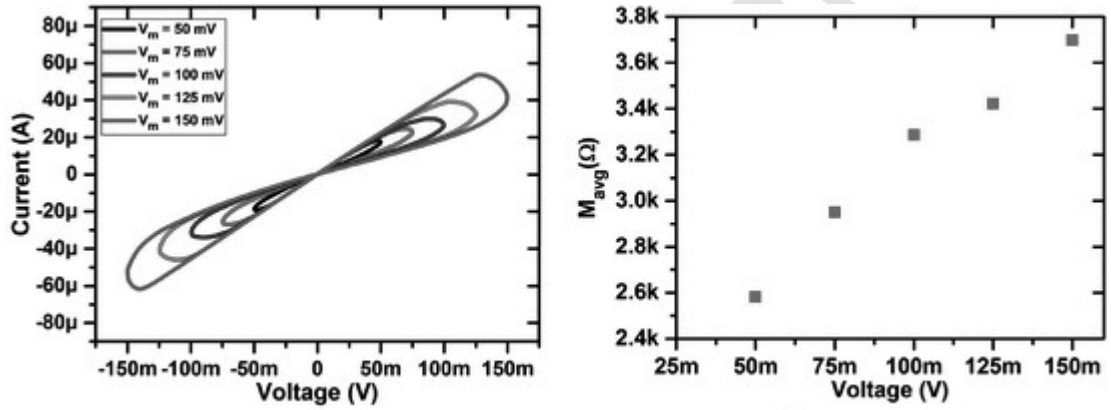
Moreover, the crucial features of the memristor emulator circuit, such as memory effect as well as incremental/decremental variation of the memristance, needs to be tested. So, to inspect these features, input pulse train having an amplitude of 100 mV, 2 μs pulse width, and 20 μs period is applied to the proposed emulator circuit. Fig. 15 shows the decremental memristance variation for different values of controlling current. It can be seen in Fig. 15(a) that during the ON time of pulse voltage excitation, the current response has increasing behavior, which implies a decremental variation of memristance, as shown in Fig. 15(b). However, the memristance value is retained in the absence of an input signal. While the results for incremental configuration are shown in Fig. 16, the current response in Fig. 16a) and memristance in Fig. 16(b) have behavior opposite to the previous one. Fig. 15 & 16 confirms the non-volatile attribute in both configurations in which the distinct curves have been obtained for the different values of controlling current, enables the proposed emulator to use as a precise controlled weight in neuromorphic circuits.

Further, the robustness of the proposed circuit has been tested in terms of signature characteristics and average memristance value for the statistical deviations in different parameters. Fig. 17 shows the Monte-Carlo simulation (1000 iterations) results for 10 %, 3σ Gaussian deviation in passive components at 1 kHz. It can be observed in Fig. 17(a) that the hysteresis curves follow the signature characteristics except for the slight variation in the loop areas, as expected. Fig. 17(b) shows the histogram plot for the sampling distribution of the average memristance value. The mean and the standard deviation has been obtained as 2581.9 $\omega$and 22.32 ω, respectively, which gives the variability (σ/μ) of 0.86%. Next, Fig. 18 shows the Mismatch analysis results using Monte-Carlo simulation (1000 runs) for 10 %, 3σ Gaussian devia-



(a) Hysteresis characteristics (b) Average memristance

Fig. 13. Electronically controllable features of the Proposed Memristor Emulator.



(a) Hysteresis characteristics (b) Average memristance

Fig. 14. Effect on memristor characteristics for different amplitude of sinusoidal excitation.

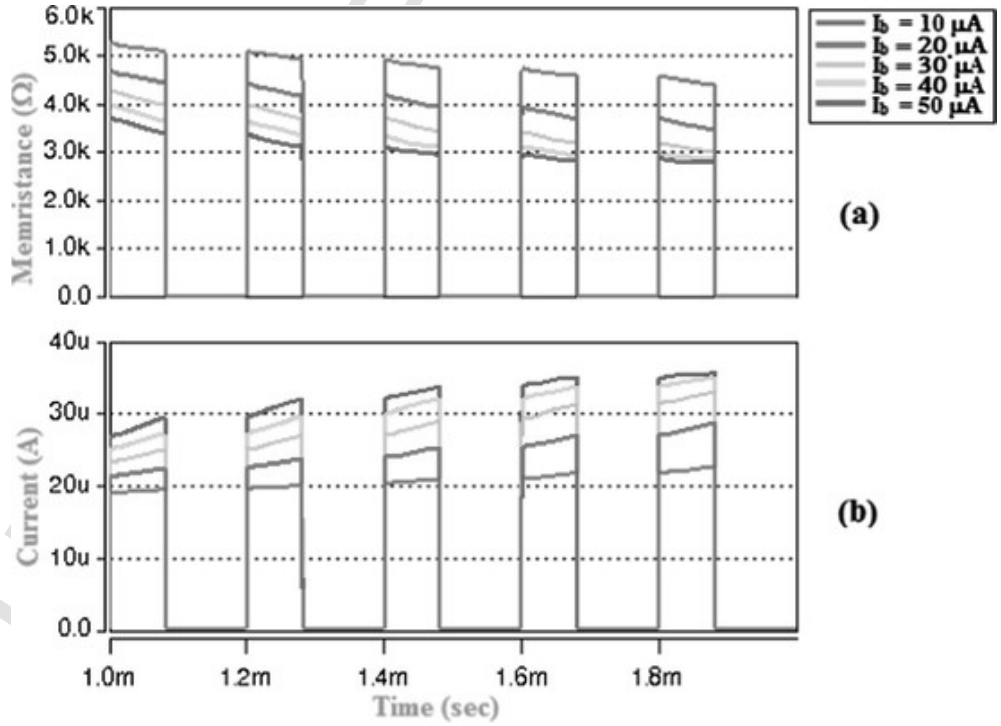


Fig. 15. Result showing non-volatile property along with its decremental Memristance variation for different I_b values.

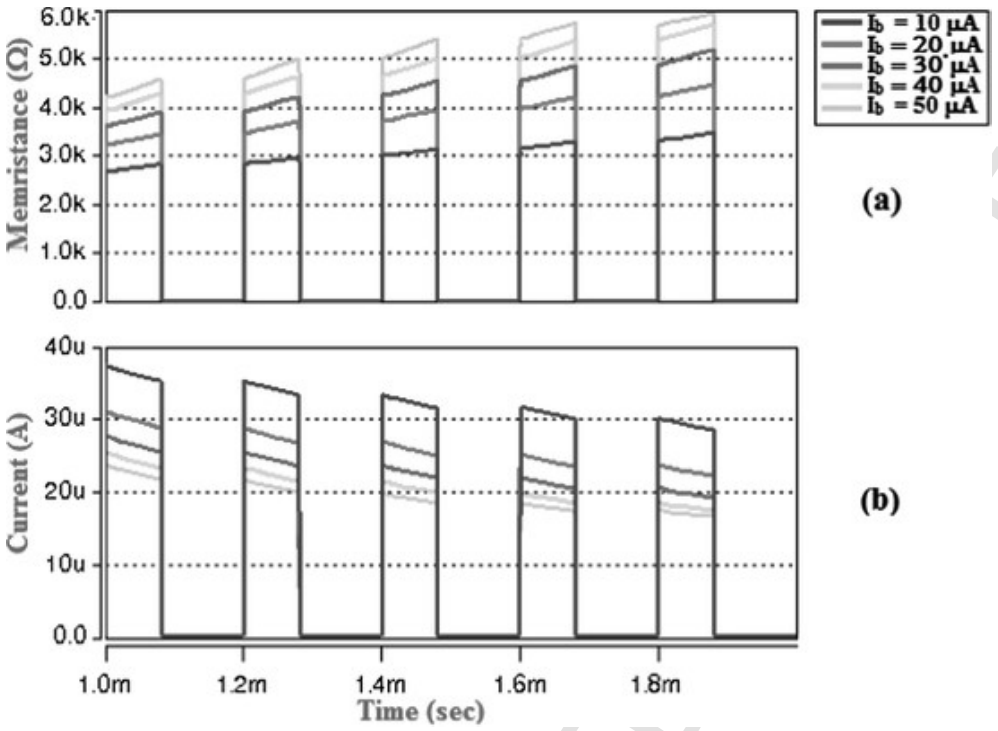


Fig. 16. Result showing non-volatile property along with its incremental Memristance variation for different values of I_b.

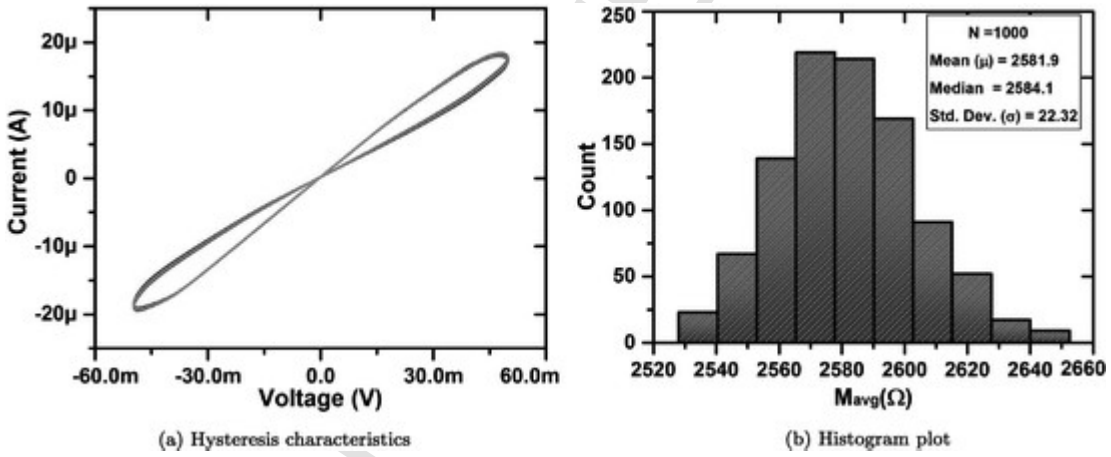


Fig. 17. Monte-Carlo simulation results for 10 % statistical variation in passive components at 1 kHz.

tion in threshold voltages of M_P, M_N at 1 kHz frequency. It can be proclaimed using Eq. (28) that the threshold mismatch may affect the constant term or the slope of the hysteresis curve without altering the signature characteristics. So, for the specified deviation, a very slight change has been observed in hysteresis characteristics shown in Fig. 18(a). The mean and the standard deviation obtained from the histogram plot in Fig. 18(b) are 2585.2 $\omega$and 1.4328 ω, which results in the variability (σ/μ) of 0.06%. Hence, it can be concluded that the assumed mismatch in threshold voltages doesn't affect the proposed design of the memristor emulator circuit. Afterward, the robustness against the statistical variation in the W/L ratio of all the MOSFETs has been estimated. Fig. 19 shows Monte-Carlo simulation result at 1 kHz for 10 %, 3σ Gaussian deviation in aspect ratios (W/L). From theoretical analysis given in Eq. (32), any mismatch in aspect ratios may affect the slope of the hysteresis curve; however, for specified deviation, it is clearly observed that all the samples are overlapped as well as follow the signature characteristics, as shown in Fig. 19(a). The mean and the standard deviation obtained from the Histogram plot in Fig. 19(b) are 2607.3 $\omega$and 35.43 ω, respectively, so the variability (σ/μ) of 1.35% has been found. So, it is concluded from the results that the proposed design is robust against different variations.

Additionally, the performance of the composite behavior of the memristor emulator circuit in parallel has been investigated. Fig. 20 illustrates the hysteresis characteristics for both the single and parallel connection of two memristors. It is found that the current varies from −41.93 μA to +41.93 μA for parallel combination and −20.96 μA to +20.96 μA for a single circuit. As expected, the equivalent memristance value in parallel combination will become half as compared to a single connection, because for the same voltage applied, the current values were exactly twice in parallel combination. Also, it is understood that the constant and the variable terms in Eq. (20) have twice value for the parallel combination, reveals that both the slope and the area of its hysteresis curve should be double in contrast to a single memristor.

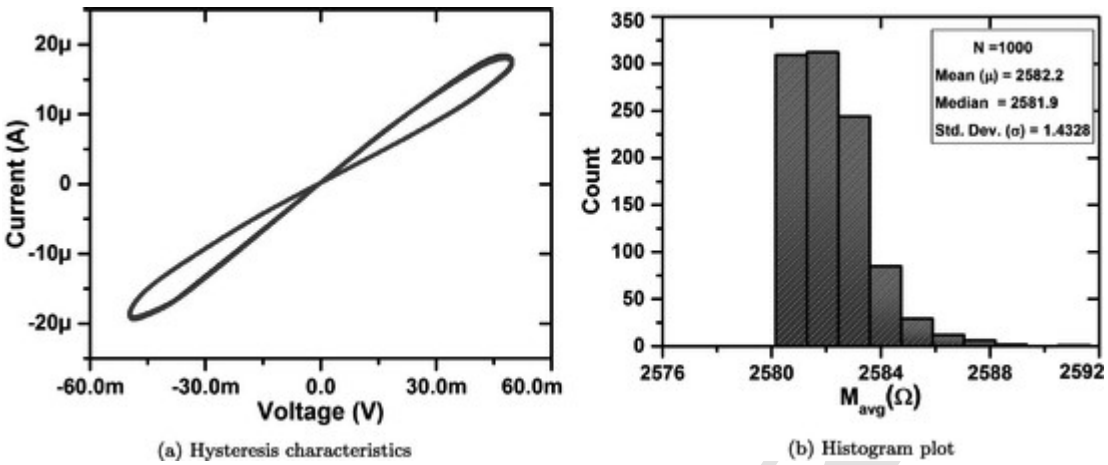


Fig. 18. Monte-Carlo simulation for 10 % statistical variation in threshold voltages of M_P, M_N.

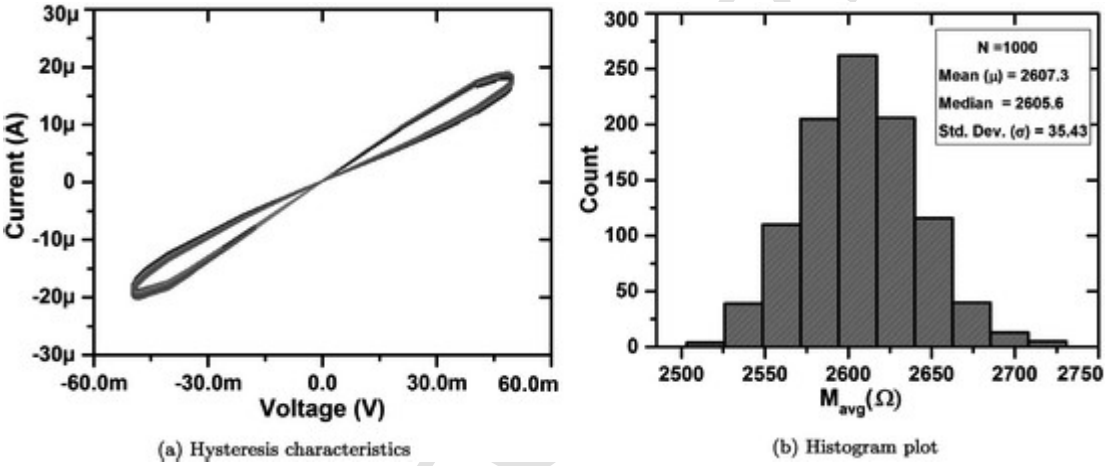


Fig. 19. Monte-Carlo simulation result for 10 % statistical variation in aspect ratio (W/L).

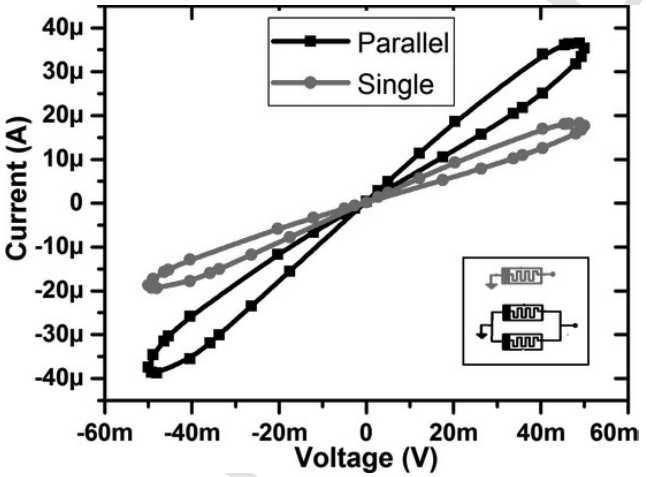


Fig. 20. Hysteresis characteristics of single and parallel combination of memristor emulators.

4. Comparison between the proposed and the existing memristor emulator circuits

The proposed memristor emulator circuit has been compared with the existing work is given in Table 3. The comparison study reveals the merits of the proposed emulator circuit.

- The memristor emulator circuits reported in [19–28,31–37,40,41,44] employs an excessive number of active building blocks, while the proposed circuit is realized using only one active element.
- The realization of the memristor emulator circuits utilize a large number of grounded [19,21–27,31,33,34,39–41,44,45] and floating [19–24,26,27,33,39,40] passive elements, whereas the proposed circuit has only one grounded capacitor.
- The realization of the memristor circuits reported in literature involves non-linear elements such as Diodes [25,33] and analog multiplier [19–24,26–28,40,41,44].
- The implementation of memristor emulators in [19–28,31,31,33,34,39–41,44] contain resistor(s) while the proposed design is resistor-less.
- Most of the existing emulator circuits either use BJT technology [19–25,27,33,34] or contains excess CMOS transistors [26,28,31,32,35–37,39,41,44,45].
- The reported memristor emulators exhibit a unique hysteresis property for a few kHz order frequency in [19–23,25,27–29,31,33,34,40,41] and near about to 1 MHz in [24,26,30,32,35–37,39,44–46]. In contrast, the proposed memristor emulator circuit can work up to 100 MHz frequencies.
- The emulator circuits reported in [20,21,27–29,33,34] can be operated only in single mode (either incremental or decremental) of memristance variation.

Table 3
Comparison between the proposed memristor emulator and the reported works in the literature.

Ref. No.	No. of active components	No. of passive components (*Grounded*)$^{\alpha}$ / (*Floating*)$^{\beta}$	Non-linear element	Resistor-less	Power supply	Transistor count	Max. operating frequency	Mode (Inc./ Dec.)	Electronic Tunability	Configurable structure
[19]	2 OPAMPs, 1 Multiplier, 10 Transistors	$(1R, 1C)^{\alpha}$ $(1R)^{\beta}$	Yes	No	±5 V	BJT	800 Hz	Dual	No	No
[20]	3 OPAMPs, 2 Multiplier	$(-)^{\alpha}$ $(5R, 1C)^{\beta}$	Yes	No	±15 V	BJT	5 kHz	Single	No	No
[21]	4 CCIIs (AD844), 1 multiplier (AD633)	$(3R, 1C)^{\alpha}$ $(2R)^{\beta}$	Yes	No	±10 V	BJT	20.2 kHz	Single	No	No
[22]	2 CCIIs (AD844), 1 multiplier (AD633), 1 buffer (TL082)	$(2R, 1C)^{\alpha}$ $(1R)^{\beta}$	Yes	No	±10 V	BJT	1 kHz	Dual	No	No
[23]	2 CCIIs (AD844), 1 multiplier (AD633)	$(1R, 1C)^{\alpha}$ $(1R)^{\beta}$	Yes	No	±10 V	BJT	160 kHz	Dual	No	No
[24]	1 CCIIs (AD844), 1 multiplier (AD633)	$(1C)^{\alpha}$ $(1R)^{\beta}$	Yes	No	±10 V	BJT	860 kHz	Dual	No	No
[25]	3 CFOAs (AD844), 1 Diode	$(2R, 2C)^{\alpha}$ $(2R)^{\beta}$	Yes	No	–	BJT	1 kHz	Dual	No	No
[26]	1 DDCC, 1 multiplier	$(1R, 1C)^{\alpha}$ $(-)^{\beta}$	Yes	No	±1.5 V	50	1 MHz	Dual	No	No
[27]	12 OTAs, 1 multiplier	$(1R, 1C)^{\alpha}$ $(2R)^{\beta}$	Yes	No	±10 V	BJT	1 kHz	Single	No	No
[28]	1 MO-OTA, 1 multiplier	$(-)^{\alpha}$ $(1R, 1C)^{\beta}$	Yes	No	± 1.25 V/ ±5 V	38	5 kHz	Single	No	No
[29]	1 OTA, 2 MOS	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±1 V	16	30 Hz	Single	No	No
[30]	1 MO-OTA	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±0.9 V	17	1 MHz	Dual	No	No
[31]	4 MO-OTA	$(3R, 1C)^{\alpha}$ $(-)^{\beta}$	No	No	±2.5 V	92	500 kHz	Dual	Yes	No
[32]	2 DO-OTA	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±1.2 V	34	8 MHz	Dual	Yes	No
[33]	4 CCII, 3 OTA	$(3R, 1C)^{\alpha}$ $(3R)^{\beta}$	No	No	±15 V	BJT	10 kHz	Single	Yes	No
[34]	2 CFOAs (AD844), 1 OTA (LM3080)	$(3R, 2C)^{\alpha}$ $(-)^{\beta}$	No	No	±12 V	BJT	2 kHz	Single	No	No
[35]	1 CDTA, 1 OTA	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±0.9 V	36	2 MHz	Dual	Yes	No
[36]	1 CDBA, 1 OTA	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±0.9 V	28	1 MHz	Dual	No	No
[37]	1 DVCC, 1 DO-OTA, 2 MOS	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±0.9 V	29	1 MHz	Dual	Yes	No
[39]	1 DVCCTA	$(2R, 1C)^{\alpha}$ $(1R)^{\beta}$	No	No	± 1.25 V	29	1 MHz	Dual	Yes	No
[40]	1 CBTA, 1 Multiplier	$(1R, 1C)^{\alpha}$ $(1R)^{\beta}$	Yes	No	±0.9 V	23	460 kHz	Dual	Yes	No
[41]	1 CCDDCC, 1 multiplier	$(1R, 1C)^{\alpha}$ $(-)^{\beta}$	Yes	No	± 1.25 V	27	100 kHz	Dual	Yes	No
[44]	1 VDTA, 1 multiplier	$(2R, 1C)^{\alpha}$ $(-)^{\beta}$	Yes	No	±0.9 V	32	2 MHz	Dual	Yes	No
[45]	1 CBTA	$(2C)^{\alpha}$ $(-)^{\beta}$	No	Yes	± 1.25 V	31	1 MHz	Dual	No	No
[46]	1 VDCC, 2 MOS	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±0.9 V	24	2 MHz	Dual	Yes	No
Proposed circuit	1 CDTA, 4 MOS	$(1C)^{\alpha}$ $(-)^{\beta}$	No	Yes	±1.2 V	24	100 MHz	Dual	Yes	Yes

- The reported work in [19–30,34,36,45] lags in terms of electronic control, while the proposed circuit can electronically control the area of hysteresis curve and memristance value.

5. Application example

To validate the proposed memristor emulator circuit, the memristor-based Schmitt-trigger and high-pass filter circuits are illustrated in Fig. 21 (a) and 22 (a), respectively. Both the circuits are obtained after replacing resistor with the proposed memristor emulator in the conventional OP-Amp based Schmitt-trigger as well as in RC-based High-pass filter. Fig. 21 (b) shows the transfer characteristics of the proposed Schmitt-trigger for different values of controlling current (I_b). Fig. 22 (b) and (c) shows the AC and transient response of the proposed MC High-pass filter. The results obtained for both the example circuits are agreed well with the theoretical assumptions.

6. Modified memristor emulator circuit

To make the design fully active, the proposed memristor emulator circuit shown in Fig. 4 is modified in Fig. 23. For this arrangement, the capacitor was removed and the terminals X+ or X− were directly connected at the gate terminal of transistor M_N. The parasitic capacitance of X+/X− terminal has been utilized in the place of external capacitor. So, for the modified memristor emulator circuit, the current–voltage relationship and the memductance in decremental configuration are modified as

$$I_{in} = \left[\left(K_N \frac{W}{L} V_G + \frac{1 + sR_Z C_Z}{R_Z}\right) - K_N \frac{W}{L} \cdot \frac{g_m R_{X-}}{(1 + sR_{X-} C_{X-})} V_{in}\right] V_{in} \tag{50}$$

$$W(\phi) = \left(K_N \frac{W}{L} V_G + \frac{1 + sR_Z C_Z}{R_Z}\right) - K_N \frac{W}{L} \cdot \frac{g_m R_{X-}}{(1 + sR_{X-} C_{X-})} V_{in} \tag{51}$$

similarly, the modified expressions in incremental configuration are

$$I_{in} = \left[\left(K_N \frac{W}{L} V_G + \frac{1 + sR_Z C_Z}{R_Z}\right) + K_N \frac{W}{L} \cdot \frac{g_m R_{X+}}{(1 + sR_{X+} C_{X+})} V_{in}\right] V_{in} \tag{52}$$

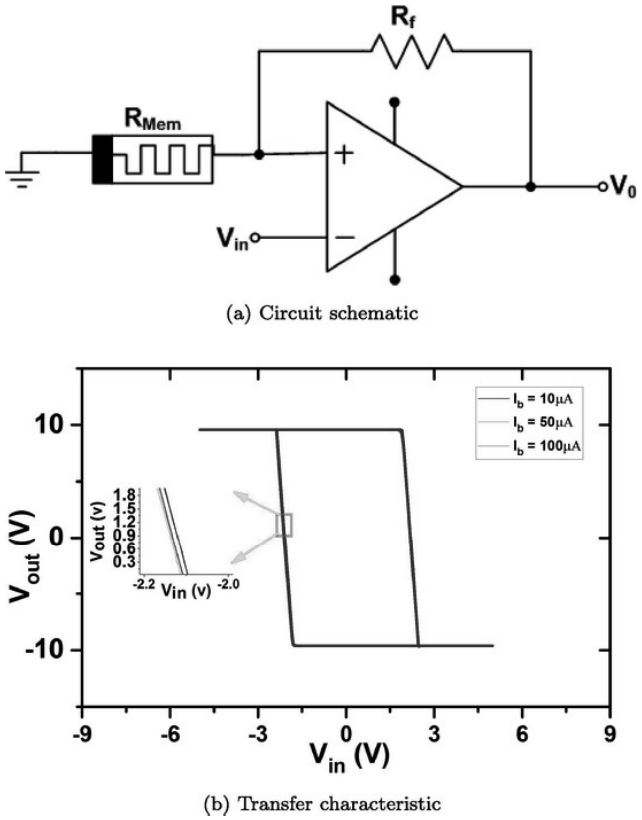


Fig. 21. Memristor-based Schmitt-trigger.

$$W(\phi) = \left(K_N \frac{W}{L} V_G + \frac{1 + sR_Z C_Z}{R_Z}\right) + K_N \frac{W}{L} \cdot \frac{g_m R_{X+}}{(1 + sR_{X+} C_{X+})} V_{in} \quad (53)$$

To verify the theoretical analysis, the proposed modified circuit is simulated at different higher frequencies. Fig. 24 demonstrates the results for the decremental configuration at the frequencies of 5 M, 10 M, 20 M and 40 MHz. From Eq. (50), it can be noted that the time-varying term affected due to the parasitic resistance R_{X-} observed in parallel with C_{X-}, which results in unsymmetrical hysteresis characteristics. However, it is managed by adjusting the controlling current (I_b), as shown in Fig. 24(a)-(d). From the results, it is revealed that this proposed circuit follows the signature characteristics for the defined range of frequencies.

7. Conclusion

This paper presents a novel Four Quadrant Analog Multiplier (FQAM) circuit and its applications using a single active element Current Differencing Transconductance Amplifier (CDTA) and two NMOS. This circuit has a cascadability feature as it produces current and voltage outputs at high and low impedance ports, respectively. It offers additional features such as resistor-less realization, operability in voltage and trans-conductance mode, and configurable structure. Further, the FQAM circuit is configured to develop a memristor emulator based on the proposed mathematical analogy. The proposed memristor circuit contains active elements (one CDTA, two NMOS, and one Inverting Voltage buffer) and only one grounded capacitor. It offers tunability using the transconductance gain of the CDTA block. Also, the proposed memristor emulator circuit doesn't contain any additional multiplier block. The emulator circuit can be operated in both the Incremental and the Decremental mode of memristance variation. It is shown that the CDTA simplifies the design of the proposed circuits and offers good operational performance. The non-idealities and signal limitation calculations are given for the proposed circuits, providing guidelines to satisfactory operating conditions. The simulation results verify the theoretical claims. In conclusion, the reported circuits contain active elements only; thus, it is suitable for IC implementation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This research is supported by Visvesvaraya Ph.D scheme under the Ministry of Electronics & Information Technology (MeitY) Government of India.

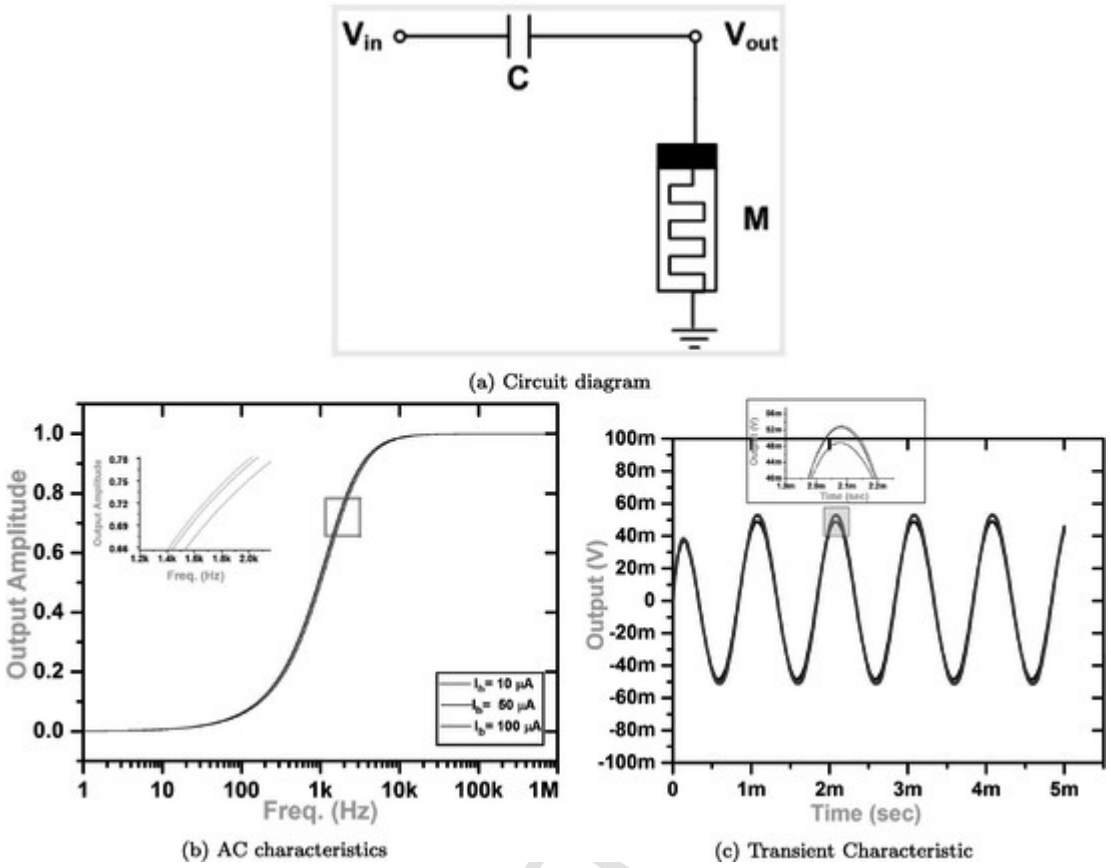


Fig. 22. MC High-pass filter.

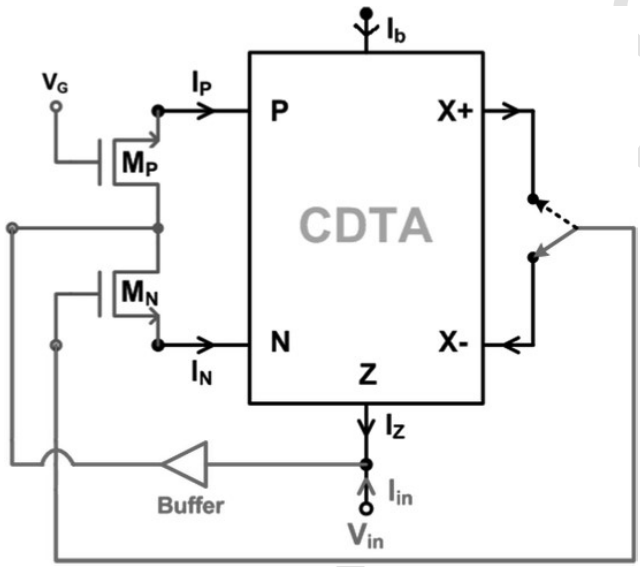


Fig. 23. Proposed Capacitor-less Memristor Emulator Circuit.

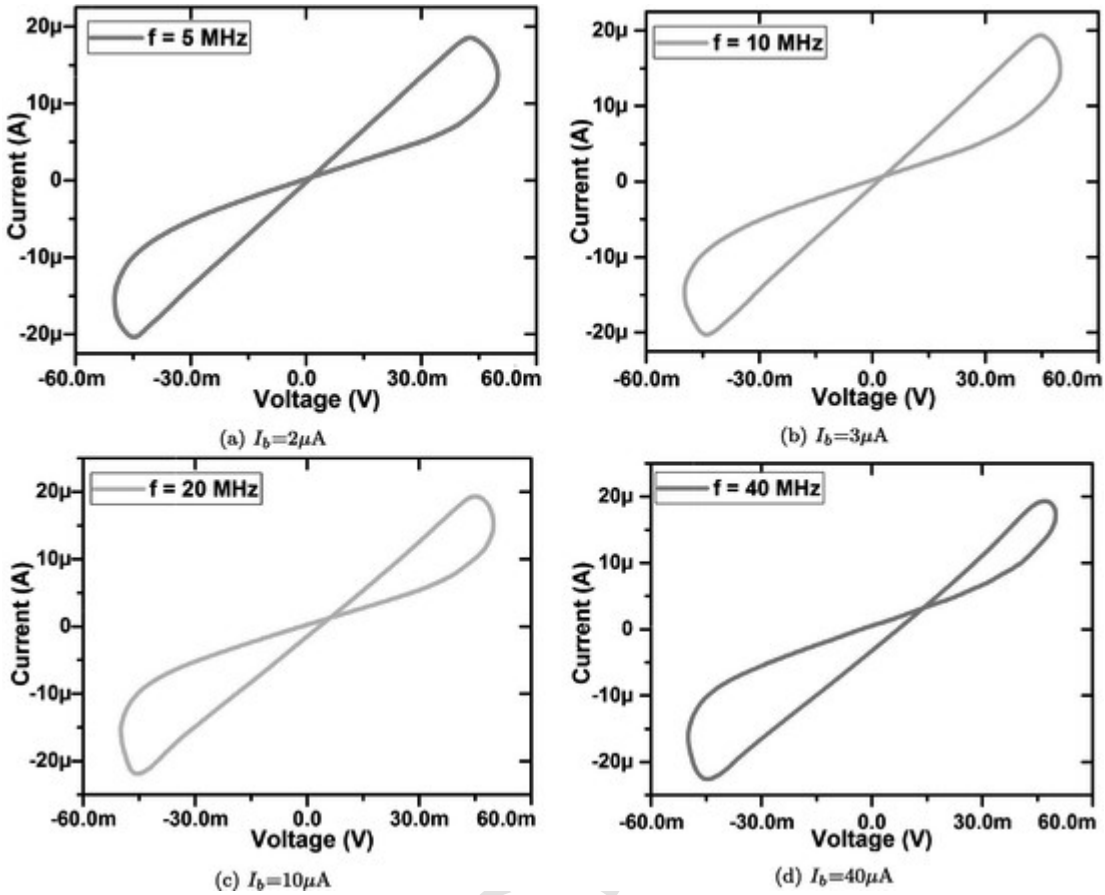


Fig. 24. Hysteresis characteristics for the proposed capacitor-less memristor emulator.

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